**VERY LARGE SCALE INTEGRATION OCTOBER MINOR PROJECT**

**NAME :** **Jaidhev Anandhev**

**BATCH MONTH : October - November Batch**

**TITLE :** **Synthesis and simulation of FIFO Architecture**

**ABSTRACT :**

This is a major project based on the concept of FIFO architecture and this project is about synthesis and simulation of FIFO Architecture. FIFO stands for First In First Out.First-in first-out memories (FIFOs) have progressed from fairly simple logic functions to high-speed buffers incorporating large blocks of SRAM. The first part presents the different functions of FIFOs and the resulting types that are found. The second part deals with current FIFO architectures and the different ways in which they work.

**INTRODUCTION :**

**WHAT EXACTLY IS FIFO IN VLSI?**

A FIFO is a special type of buffer. The name FIFO stands for first in first out and means that the data written into the buffer first comes out of it first. There are other kinds of buffers like the LIFO (last in first out), often called a stack memory, and the shared memory. The choice of a buffer architecture depends on the application to be solved. FIFOs are used in designs to safely pass multi-bit data words from one clock domain to another, or to control the flow of data between source and destination sides sitting in the same clock domain. If read and write clock domains are governed by the same clock signal, FIFO is said to be synchronous.FIFO is an approach for handling program work requests from queues or stacks so that the oldest request is handled first. In hardware, it is either an array of flops or read/write memory that stores data from one clock domain and on request supplies the same data to other clock domains following FIFO logic.

**FIFO TYPES:**

**THERE ARE THREE KINDS OF FIFO:**

• Shift register – FIFO with an invariable number of stored data words and, thus, the necessary synchronism between

the read and the write operations because a data word must be read every time one is written

• Exclusive read/write FIFO – FIFO with a variable number of stored data words and, because of the internal structure,

the necessary synchronism between the read and the write operations

• Concurrent read/write FIFO – FIFO with a variable number of stored data words and possible asynchronism

between the read and the write operation

**WORKING OF FIFO :**

In FIFO, the data which is stored first is taken out first. It is an exclusive read and write operation.

FIFO is an approach for handling program work requests from queues or stacks so that the oldest request is handled first. In hardware, it is either an array of flops or read/write memory that stores data from one clock domain and on request supplies the same data to other clock domains following FIFO logic.

Clock domain that supplies data to FIFO is often referred to as write or input logic, and the clock domain that reads data from FIFO is often referred to as read or output logic.

**EXCLUSIVE READ/WRITE FIFOS:**

In exclusive read/write FIFOs, the writing of data is not independent of how the data is read. There are timing relationships between the write clock and the read clock. For instance, overlapping of the read and the write clocks could be prohibited. To permit use of such FIFOs between two systems that work asynchronously to one another, an external circuit is required for synchronization. But this synchronization circuit usually considerably reduces the data rate.

**CONCURRENT READ / WRITE FIFO :**

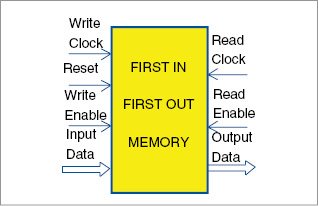
In concurrent read/write FIFOs, there is no dependence between the writing and reading of data. Simultaneous writing and reading are possible in overlapping fashion or successively. This means that two systems with different frequencies can be

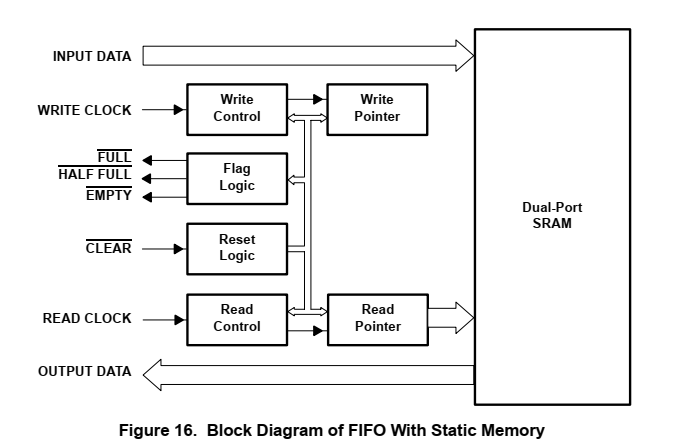
connected to the FIFO. The designer need not worry about synchronizing the two systems because this is taken care of in the FIFO. Concurrent read/write FIFOs, depending on the control signals for writing and reading, fall into two groups:

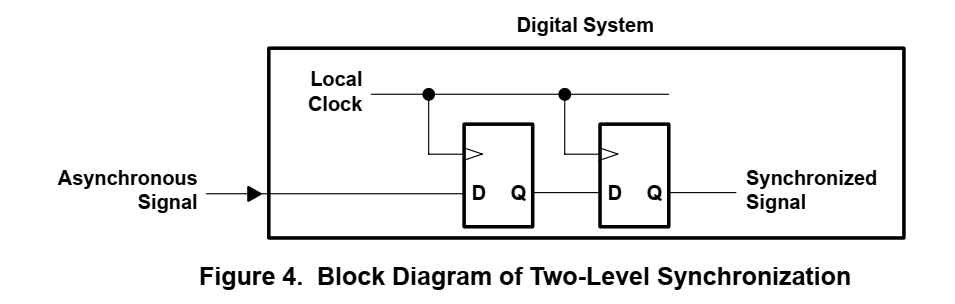
• Synchronous FIFOs

• Asynchronous FIFOs

**BLOCK DIAGRAM :**







**ASYNCHRONOUS FIFOS :**

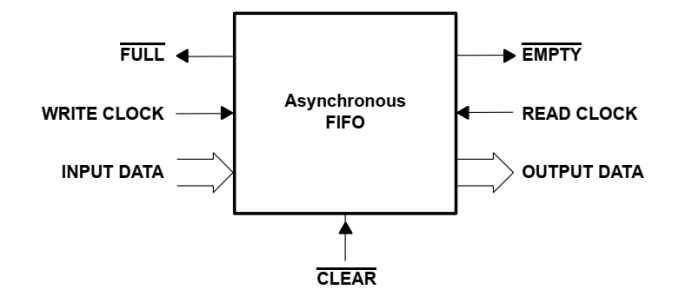
In aynchronous flip flop there are two types of signals they are full and empty. Full signal represents that the FIFO is completed / data is completely filled inside the data. An empty signal represents that there is no data in the memory.

Write clock represents the data that should be written into the memory. The Read clock represents the data that should be read from the memory.

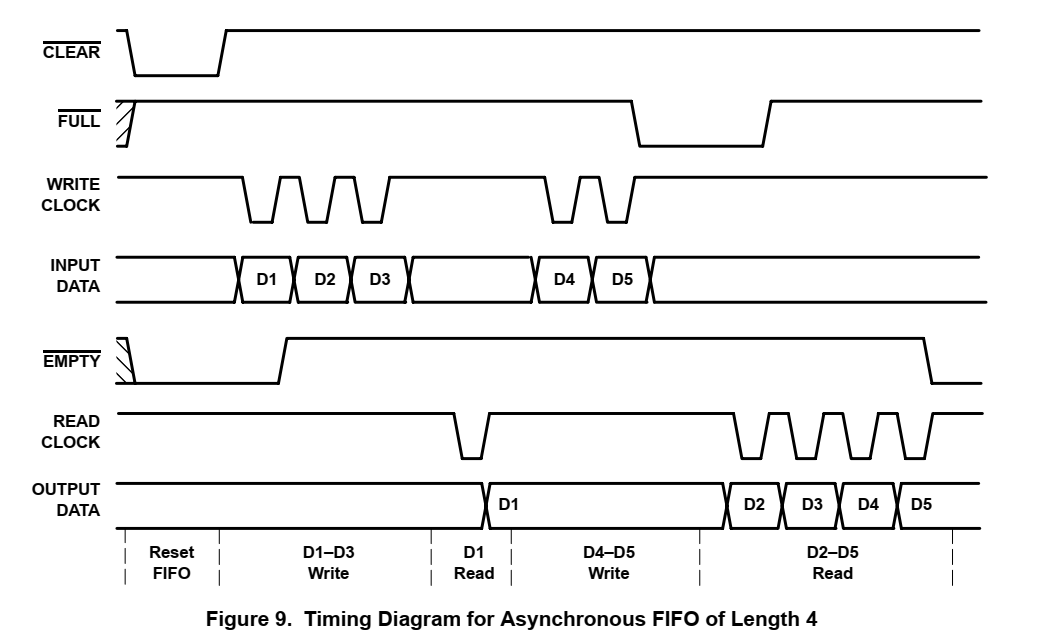
Input data represents the data that has to be written into the memory by taking write clock. Output data reads the data from the read clock.

Therefore, it is analyzed that when the write clock is high , input data is taken and when the read clock is high, output data is given.

**BLOCK DIAGRAM OF ASYNCHRONOUS FIFO :**

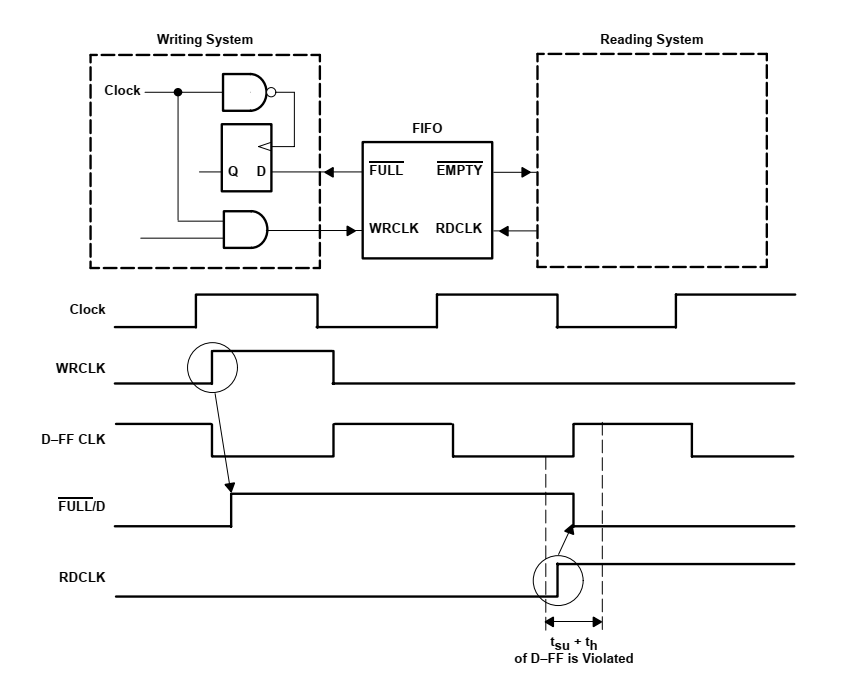


**TIMING DIAGRAM :**



* When the write clock is high and read clock is also high, the output data is in RESET FIFO state.
* When write clock is low which means that the input data is given and read clock is high, the output data is in Write state.
* When the write clock is high such that no input data is given and read clock is high it means that the output data is in write state.

**MICROARCHITECTURE OF THE CIRCUIT :**



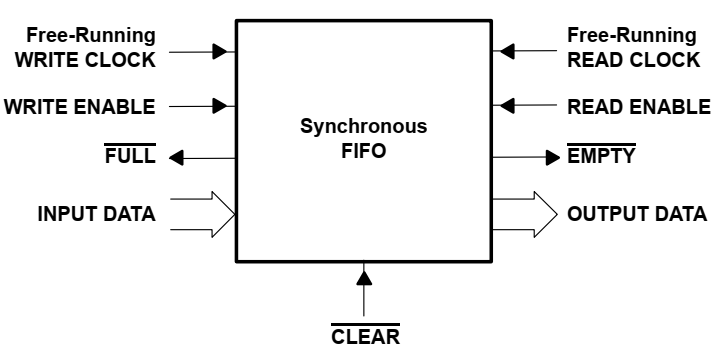
**SYNCHRONOUS FIFO :**

Synchronous FIFOs are controlled based on methods of control proven in processor systems. Every digital processor system works synchronized with a system-wide clock signal. This system timing continues to run even if no actions are being executed.

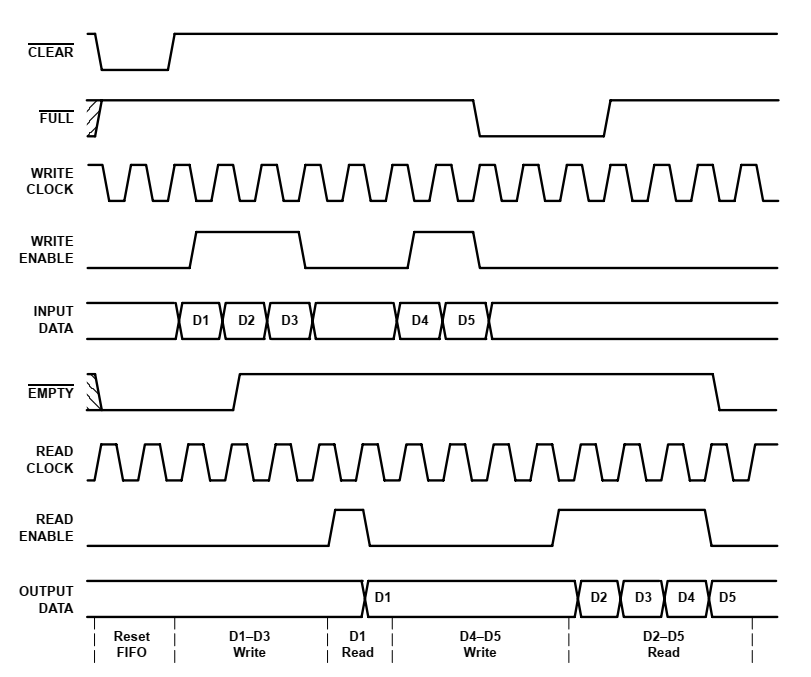
In synchronous clock the write clock is free-running and read clock is also free-running.

Write clock represents the data should be written into the memory. Read clock represents the data should be read from the memory which is similar to asynchronous mode.

**BLOCK DIAGRAM OF FIFO :**



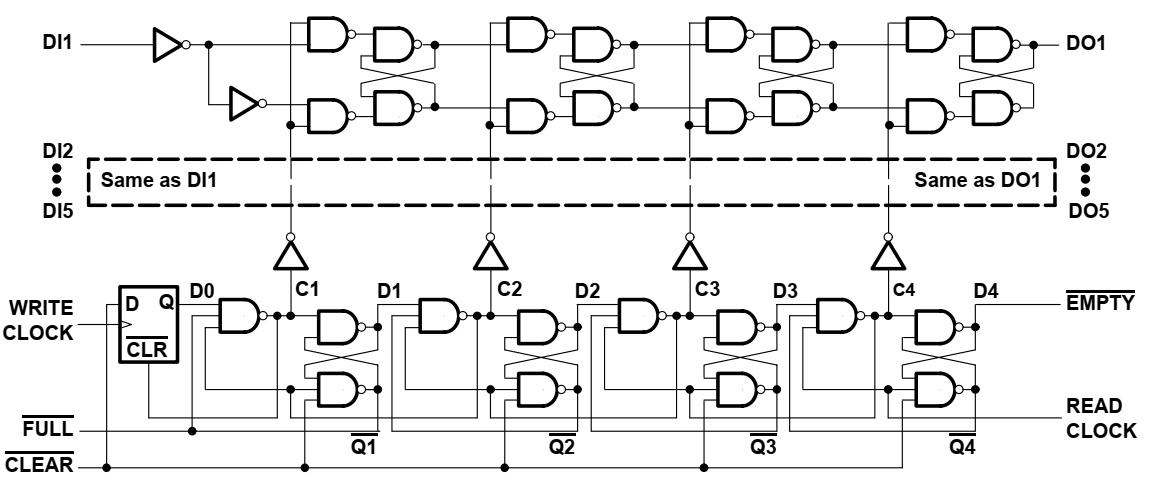
**TIMING DIAGRAM :**

****

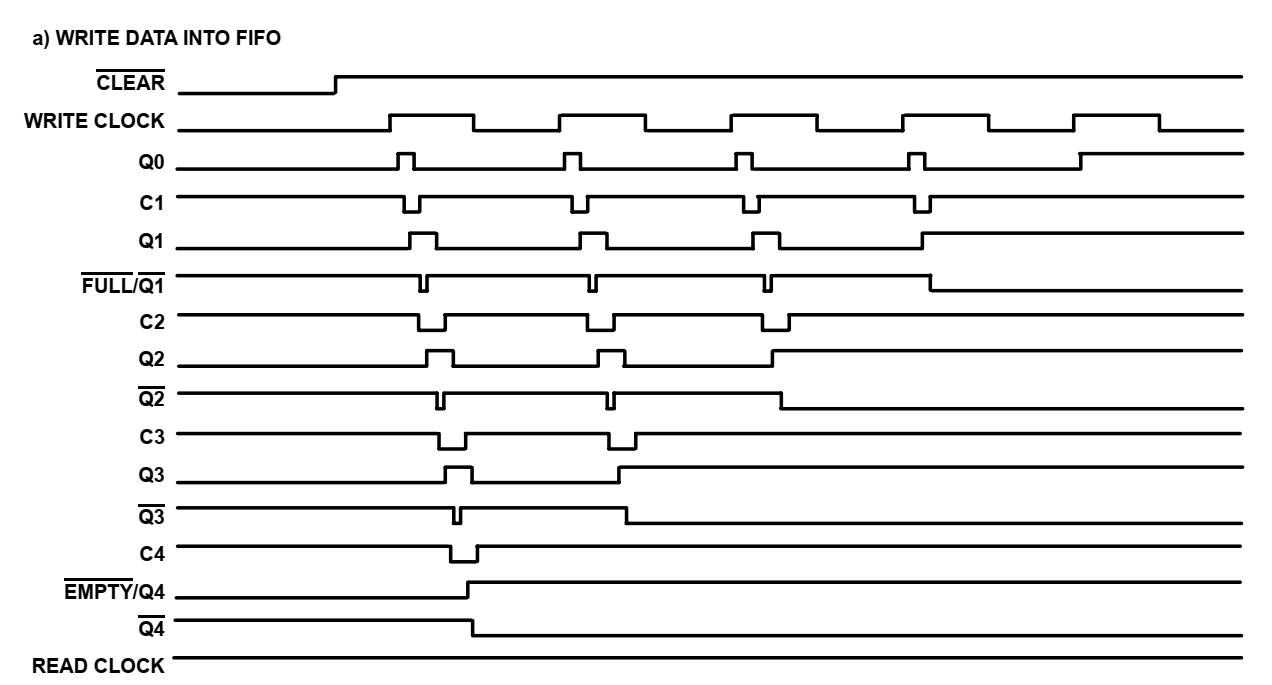
* From the timing diagram , it is clear that when both write enable and read enable is low, the output is in reset FIFO state.
* When write enable is high, that is input data is given and read enable is low the output is in write state.
* When write clock is low, no input data is given and read clock is high the output is in read state.

**FIFO ARCHITECTURES :**

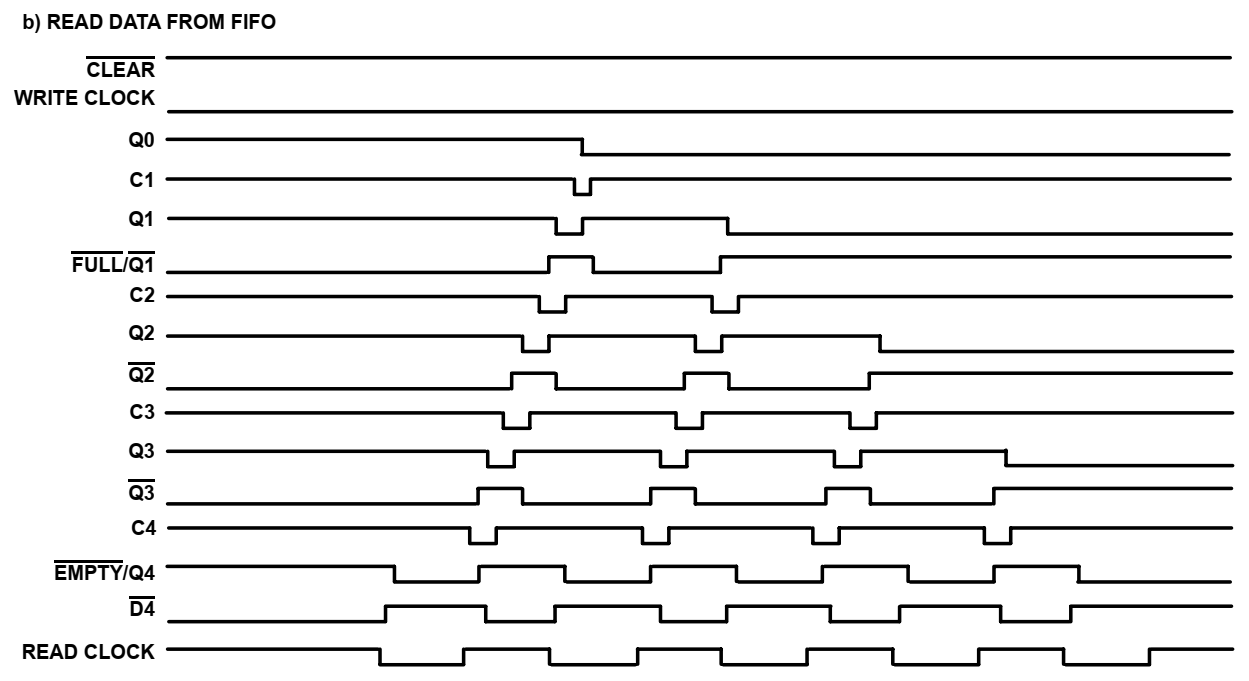
All the kinds of FIFOs described in FIFO Types can be implemented in different hardware architectures. The architecture of conventional FIFOs has constantly been developed. Initially, FIFOs worked by the fall-through principle. Today, FIFOs are nearly always based on an SRAM, which produced a considerable increase in the number of data words stored, despite the faster speed. All possible hardware architectures also are found in software FIFOs



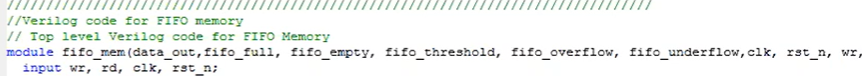
**TIMING DIAGRAM FOR WRITE DATA IN FIFO :**



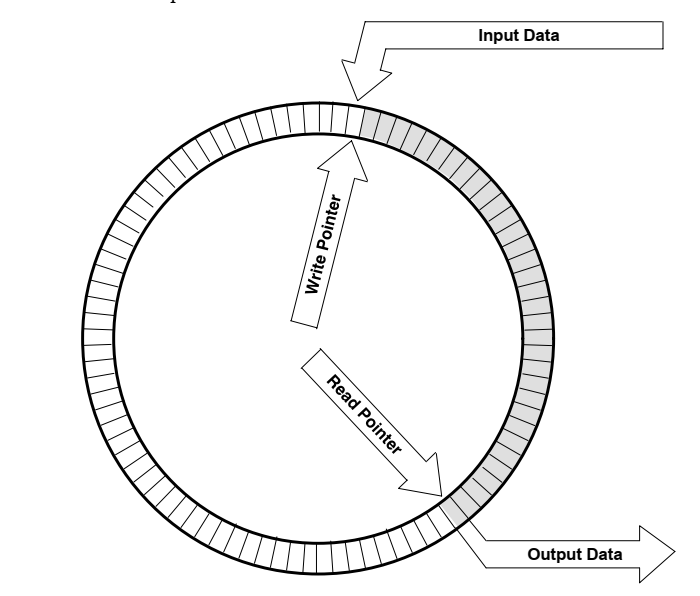
**TIMING DIAGRAM FOR READ DATA IN FIFO :**



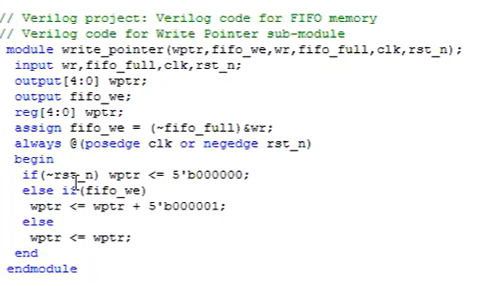
**PRINCIPLE OF CIRCULAR FIFO WITH TWO POINTERS :**



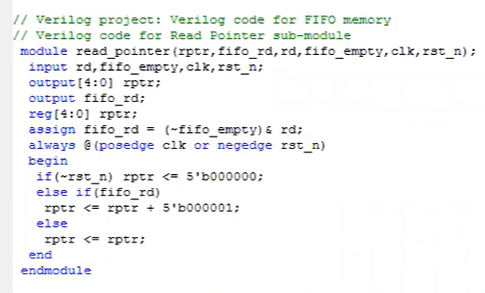
The above code is implenented based on this method given below.



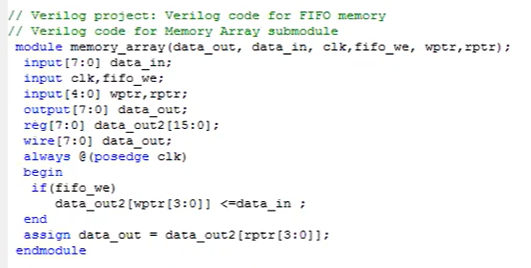
**THE WRITE CLOCK IS IMPLEMENTED USING THE CODE GIVEN BELOW :(FOR TOP 1).**



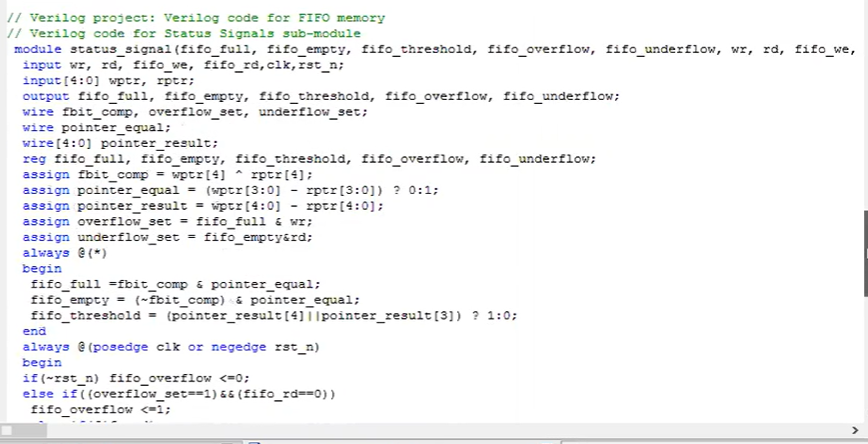
**THE READ CLOCK IS IMPLEMENTED USING THE CODE GIVEN BELOW :(FOR TOP 2).**



**THE MEMORY ARRAY IS IMPLEMENTED USING THE CODE GIVEN BELOW :(FOR TOP 3).**



**THE STATUS SIGNAL IS IMPLEMENTED USING THE CODE GIVEN BELOW :(FOR TOP 4).**



**PROJECT SUMMARY :**

|  |  |  |  |
| --- | --- | --- | --- |
| fifo\_mem Project Status (12/16/2022 - 18:14:51) | | | |
| Project File: | Major\_Project\_VLSI.xise | Parser Errors: | No Errors |
| Module Name: | fifo\_mem | Implementation State: | Placed and Routed |
| Target Device: | xc7a100t-3csg324 | Errors: | No Errors |
| Product Version: | ISE 14.7 | Warnings: | [35 Warnings (4 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/*.xmsgs?&DataKey=Warning) |
| Design Goal: | Balanced | Routing Results: | [All Signals Completely Routed](C:/ISE Files/Major_Project_VLSI\\fifo_mem.unroutes) |
| Design Strategy: | [Xilinx Default (unlocked)](C:\\Users\\jayak\\AppData\\Local\\Temp\\Xilinx Default (unlocked)?&DataKey=Strategy) | Timing Constraints: | [All Constraints Met](C:/ISE Files/Major_Project_VLSI\\fifo_mem.ptwx?&DataKey=ConstraintsData) |
| Environment: | [System Settings](C:/ISE Files/Major_Project_VLSI\\fifo_mem_envsettings.html) | Final Timing Score: | 0  [(Timing Report)](C:/ISE Files/Major_Project_VLSI\\fifo_mem.twx?&DataKey=XmlTimingReport) |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Device Utilization Summary | | | | |
| Slice Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of Slice Registers | 12 | 126,800 | 1% |  |
| Number used as Flip Flops | 12 |  |  |  |
| Number used as Latches | 0 |  |  |  |
| Number used as Latch-thrus | 0 |  |  |  |
| Number used as AND/OR logics | 0 |  |  |  |
| Number of Slice LUTs | 35 | 63,400 | 1% |  |
| Number used as logic | 27 | 63,400 | 1% |  |
| Number using O6 output only | 22 |  |  |  |
| Number using O5 output only | 0 |  |  |  |
| Number using O5 and O6 | 5 |  |  |  |
| Number used as ROM | 0 |  |  |  |
| Number used as Memory | 8 | 19,000 | 1% |  |
| Number used as Dual Port RAM | 8 |  |  |  |
| Number using O6 output only | 4 |  |  |  |
| Number using O5 output only | 0 |  |  |  |
| Number using O5 and O6 | 4 |  |  |  |
| Number used as Single Port RAM | 0 |  |  |  |
| Number used as Shift Register | 0 |  |  |  |
| Number used exclusively as route-thrus | 0 |  |  |  |
| Number of occupied Slices | 12 | 15,850 | 1% |  |
| Number of LUT Flip Flop pairs used | 35 |  |  |  |
| Number with an unused Flip Flop | 27 | 35 | 77% |  |
| Number with an unused LUT | 0 | 35 | 0% |  |
| Number of fully used LUT-FF pairs | 8 | 35 | 22% |  |
| Number of unique control sets | 5 |  |  |  |
| Number of slice register sites lost         to control set restrictions | 24 | 126,800 | 1% |  |
| Number of bonded [IOBs](C:/ISE Files/Major_Project_VLSI\\fifo_mem_map.xrpt?&DataKey=IOBProperties) | 25 | 210 | 11% |  |
| Number of RAMB36E1/FIFO36E1s | 0 | 135 | 0% |  |
| Number of RAMB18E1/FIFO18E1s | 0 | 270 | 0% |  |
| Number of BUFG/BUFGCTRLs | 1 | 32 | 3% |  |
| Number used as BUFGs | 1 |  |  |  |
| Number used as BUFGCTRLs | 0 |  |  |  |
| Number of IDELAYE2/IDELAYE2\_FINEDELAYs | 0 | 300 | 0% |  |
| Number of ILOGICE2/ILOGICE3/ISERDESE2s | 0 | 300 | 0% |  |
| Number of ODELAYE2/ODELAYE2\_FINEDELAYs | 0 |  |  |  |
| Number of OLOGICE2/OLOGICE3/OSERDESE2s | 0 | 300 | 0% |  |
| Number of PHASER\_IN/PHASER\_IN\_PHYs | 0 | 24 | 0% |  |
| Number of PHASER\_OUT/PHASER\_OUT\_PHYs | 0 | 24 | 0% |  |
| Number of BSCANs | 0 | 4 | 0% |  |
| Number of BUFHCEs | 0 | 96 | 0% |  |
| Number of BUFRs | 0 | 24 | 0% |  |
| Number of CAPTUREs | 0 | 1 | 0% |  |
| Number of DNA\_PORTs | 0 | 1 | 0% |  |
| Number of DSP48E1s | 0 | 240 | 0% |  |
| Number of EFUSE\_USRs | 0 | 1 | 0% |  |
| Number of FRAME\_ECCs | 0 | 1 | 0% |  |
| Number of IBUFDS\_GTE2s | 0 | 4 | 0% |  |
| Number of ICAPs | 0 | 2 | 0% |  |
| Number of IDELAYCTRLs | 0 | 6 | 0% |  |
| Number of IN\_FIFOs | 0 | 24 | 0% |  |
| Number of MMCME2\_ADVs | 0 | 6 | 0% |  |
| Number of OUT\_FIFOs | 0 | 24 | 0% |  |
| Number of PCIE\_2\_1s | 0 | 1 | 0% |  |
| Number of PHASER\_REFs | 0 | 6 | 0% |  |
| Number of PHY\_CONTROLs | 0 | 6 | 0% |  |
| Number of PLLE2\_ADVs | 0 | 6 | 0% |  |
| Number of STARTUPs | 0 | 1 | 0% |  |
| Number of XADCs | 0 | 1 | 0% |  |
| Average Fanout of Non-Clock Nets | 3.79 |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Performance Summary | | | |
| Final Timing Score: | 0 (Setup: 0, Hold: 0) | Pinout Data: | [Pinout Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem_par.xrpt?&DataKey=PinoutData) |
| Routing Results: | [All Signals Completely Routed](C:/ISE Files/Major_Project_VLSI\\fifo_mem.unroutes) | Clock Data: | [Clock Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem_par.xrpt?&DataKey=ClocksData) |
| Timing Constraints: | [All Constraints Met](C:/ISE Files/Major_Project_VLSI\\fifo_mem.ptwx?&DataKey=ConstraintsData) |  |  |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Detailed Reports | | | | | |
| Report Name | Status | Generated | Errors | Warnings | Infos |
| [Synthesis Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem.syr) | Current | Fri Dec 16 18:14:07 2022 | 0 | [4 Warnings (4 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/xst.xmsgs?&DataKey=Warning) | [1 Info (1 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/xst.xmsgs?&DataKey=Info) |
| [Translation Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem.bld) | Current | Fri Dec 16 18:14:14 2022 | 0 | 0 | 0 |
| [Map Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem_map.mrp) | Current | Fri Dec 16 18:14:31 2022 | 0 | [28 Warnings (0 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/map.xmsgs?&DataKey=Warning) | [7 Infos (0 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/map.xmsgs?&DataKey=Info) |
| [Place and Route Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem.par) | Current | Fri Dec 16 18:14:43 2022 | 0 | [3 Warnings (0 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/par.xmsgs?&DataKey=Warning) | [3 Infos (0 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/par.xmsgs?&DataKey=Info) |
| Power Report |  |  |  |  |  |
| [Post-PAR Static Timing Report](C:/ISE Files/Major_Project_VLSI\\fifo_mem.twr) | Current | Fri Dec 16 18:14:51 2022 | 0 | 0 | [4 Infos (0 new)](C:/ISE Files/Major_Project_VLSI\\_xmsgs/trce.xmsgs?&DataKey=Info) |
| Bitgen Report |  |  |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| Secondary Reports | | | [[-]](C:\\Users\\jayak\\AppData\\Local\\Temp\\?&ExpandedTable=SecondaryReports) |
| Report Name | Status | Generated | |
| [ISIM Simulator Log](C:/ISE Files/Major_Project_VLSI\\isim.log) | Out of Date | Fri Dec 16 17:51:00 2022 | |

Date Generated: 12/16/2022 - 19:24:47

**IOB PROPERTIES :**

IOB Properties  -  Fri Dec 16 19:31:09 2022

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| IOB Name | Type | Direction | IO Standard | Diff Term | Drive Strength | Slew Rate | Reg (s) | Resistor | IOB Delay |
| clk | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<0> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<1> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<2> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<3> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<4> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<5> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<6> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_in<7> | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| data\_out<0> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<1> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<2> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<3> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<4> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<5> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<6> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| data\_out<7> | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| fifo\_empty | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| fifo\_full | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| fifo\_overflow | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| fifo\_threshold | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| fifo\_underflow | IOB | OUTPUT | LVCMOS18 |  | 12 | SLOW |  |  |  |
| rd | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| rst\_n | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |
| wr | IOB | INPUT | LVCMOS18 |  |  |  |  |  |  |

**TIMING CONSTRAINTS:**

--------------------------------------------------------------------------------

Release 14.7 Trace (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3

-n 3 -fastpaths -xml fifo\_mem.twx fifo\_mem.ncd -o fifo\_mem.twr fifo\_mem.pcf

Design file: fifo\_mem.ncd

Physical constraint file: fifo\_mem.pcf

Device,package,speed: xc7a100t,csg324,C,-3 (PRODUCTION 1.10 2013-10-13)

Report level: verbose report

Environment Variable Effect

-------------------- ------

NONE No environment variables were set

--------------------------------------------------------------------------------

INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the [Timing Closure User Guide (UG612).](C:\\Users\\jayak\\AppData\\Local\\Temp\\infoHelpLink^UG612)

INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths

option. All paths that are not constrained will be reported in the

unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on

a 50 Ohm transmission line loading model. For the details of this model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

-----------------

All values displayed in nanoseconds (ns)

Setup/Hold to clock clk

------------+------------+------------+------------+------------+------------------+--------+

|Max Setup to| Process |Max Hold to | Process | | Clock |

Source | clk (edge) | Corner | clk (edge) | Corner |Internal Clock(s) | Phase |

------------+------------+------------+------------+------------+------------------+--------+

data\_in<0> | -0.478(R)| FAST | 2.609(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<1> | -0.496(R)| FAST | 2.617(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<2> | -0.569(R)| FAST | 2.748(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<3> | -0.524(R)| FAST | 2.634(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<4> | -0.554(R)| FAST | 2.680(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<5> | -0.497(R)| FAST | 2.619(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<6> | -0.401(R)| FAST | 2.655(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<7> | -0.417(R)| FAST | 2.715(R)| SLOW |clk\_BUFGP | 0.000|

rd | -0.003(R)| FAST | 2.304(R)| SLOW |clk\_BUFGP | 0.000|

rst\_n | 0.057(R)| FAST | 1.793(R)| SLOW |clk\_BUFGP | 0.000|

wr | 0.639(R)| FAST | 2.009(R)| SLOW |clk\_BUFGP | 0.000|

------------+------------+------------+------------+------------+------------------+--------+

Clock clk to Pad

--------------+-----------------+------------+-----------------+------------+------------------+--------+

|Max (slowest) clk| Process |Min (fastest) clk| Process | | Clock |

Destination | (edge) to PAD | Corner | (edge) to PAD | Corner |Internal Clock(s) | Phase |

--------------+-----------------+------------+-----------------+------------+------------------+--------+

data\_out<0> | 8.950(R)| SLOW | 3.639(R)| FAST |clk\_BUFGP | 0.000|

data\_out<1> | 8.811(R)| SLOW | 3.554(R)| FAST |clk\_BUFGP | 0.000|

data\_out<2> | 8.966(R)| SLOW | 3.562(R)| FAST |clk\_BUFGP | 0.000|

data\_out<3> | 8.717(R)| SLOW | 3.451(R)| FAST |clk\_BUFGP | 0.000|

data\_out<4> | 8.880(R)| SLOW | 3.511(R)| FAST |clk\_BUFGP | 0.000|

data\_out<5> | 8.782(R)| SLOW | 3.466(R)| FAST |clk\_BUFGP | 0.000|

data\_out<6> | 8.629(R)| SLOW | 3.421(R)| FAST |clk\_BUFGP | 0.000|

data\_out<7> | 8.625(R)| SLOW | 3.448(R)| FAST |clk\_BUFGP | 0.000|

fifo\_empty | 8.828(R)| SLOW | 3.554(R)| FAST |clk\_BUFGP | 0.000|

fifo\_full | 9.176(R)| SLOW | 3.694(R)| FAST |clk\_BUFGP | 0.000|

fifo\_overflow | 7.654(R)| SLOW | 3.163(R)| FAST |clk\_BUFGP | 0.000|

fifo\_threshold| 8.841(R)| SLOW | 3.436(R)| FAST |clk\_BUFGP | 0.000|

fifo\_underflow| 7.807(R)| SLOW | 3.240(R)| FAST |clk\_BUFGP | 0.000|

--------------+-----------------+------------+-----------------+------------+------------------+--------+

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 2.446| | | |

---------------+---------+---------+---------+---------+

Analysis completed Fri Dec 16 18:14:51 2022

--------------------------------------------------------------------------------

Trace Settings:

-------------------------

Trace Settings

Peak Memory Usage: 632 MB

**PINOUT REPORT :**

Pinout Report  -  Fri Dec 16 19:32:38 2022

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Pin Number | Signal Name | Pin Usage | Pin Name | Direction | IO Standard | IO Bank Number | Drive (mA) | Slew Rate | Termination | IOB Delay | Voltage | Constraint | IO Register | Signal Integrity |
| A1 |  | IOB33S | IO\_L9N\_T1\_DQS\_AD7N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| A2 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| A3 |  | IOB33S | IO\_L8N\_T1\_AD14N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| A4 |  | IOB33M | IO\_L8P\_T1\_AD14P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| A5 |  | IOB33S | IO\_L3N\_T0\_DQS\_AD5N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| A6 |  | IOB33M | IO\_L3P\_T0\_DQS\_AD5P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| A7 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| A8 |  | IOB33S | IO\_L12N\_T1\_MRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| A9 |  | IOB33S | IO\_L14N\_T2\_SRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| A10 |  | IOB33M | IO\_L14P\_T2\_SRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| A11 | data\_in<0> | IOB | IO\_L4N\_T0\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| A12 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| A13 | rd | IOB | IO\_L9P\_T1\_DQS\_AD3P\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| A14 | fifo\_empty | IOB | IO\_L9N\_T1\_DQS\_AD3N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| A15 | data\_in<7> | IOB | IO\_L8P\_T1\_AD10P\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| A16 | fifo\_threshold | IOB | IO\_L8N\_T1\_AD10N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| A17 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| A18 | fifo\_full | IOB | IO\_L10N\_T1\_AD11N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| B1 |  | IOB33M | IO\_L9P\_T1\_DQS\_AD7P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B2 |  | IOB33S | IO\_L10N\_T1\_AD15N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B3 |  | IOB33M | IO\_L10P\_T1\_AD15P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B4 |  | IOB33S | IO\_L7N\_T1\_AD6N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B5 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| B6 |  | IOB33S | IO\_L2N\_T0\_AD12N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B7 |  | IOB33M | IO\_L2P\_T0\_AD12P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| B8 |  | IOB33M | IO\_L12P\_T1\_MRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| B9 |  | IOB33S | IO\_L11N\_T1\_SRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| B10 |  |  | VCCO\_16 |  |  | 16 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| B11 | data\_out<7> | IOB | IO\_L4P\_T0\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| B12 | data\_out<6> | IOB | IO\_L3N\_T0\_DQS\_AD1N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| B13 | data\_out<3> | IOB | IO\_L2P\_T0\_AD8P\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| B14 | data\_out<4> | IOB | IO\_L2N\_T0\_AD8N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| B15 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| B16 | data\_in<5> | IOB | IO\_L7P\_T1\_AD2P\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| B17 | data\_in<6> | IOB | IO\_L7N\_T1\_AD2N\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| B18 | rst\_n | IOB | IO\_L10P\_T1\_AD11P\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| C1 |  | IOB33S | IO\_L16N\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C2 |  | IOB33M | IO\_L16P\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C3 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| C4 |  | IOB33M | IO\_L7P\_T1\_AD6P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C5 |  | IOB33S | IO\_L1N\_T0\_AD4N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C6 |  | IOB33M | IO\_L1P\_T0\_AD4P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C7 |  | IOB33S | IO\_L4N\_T0\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| C8 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| C9 |  | IOB33M | IO\_L11P\_T1\_SRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| C10 |  | IOB33S | IO\_L13N\_T2\_MRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| C11 |  | IOB33M | IO\_L13P\_T2\_MRCC\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| C12 | data\_out<5> | IOB | IO\_L3P\_T0\_DQS\_AD1P\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| C13 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| C14 | data\_out<2> | IOB | IO\_L1N\_T0\_AD0N\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| C15 |  | IOB33S | IO\_L12N\_T1\_MRCC\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| C16 |  | IOB33M | IO\_L20P\_T3\_A20\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| C17 |  | IOB33S | IO\_L20N\_T3\_A19\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| C18 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| D1 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| D2 |  | IOB33S | IO\_L14N\_T2\_SRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| D3 |  | IOB33S | IO\_L12N\_T1\_MRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| D4 |  | IOB33S | IO\_L11N\_T1\_SRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| D5 | clk | IOB | IO\_L11P\_T1\_SRCC\_35 | INPUT | LVCMOS18\* | 35 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| D6 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| D7 |  | IOB33S | IO\_L6N\_T0\_VREF\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| D8 |  | IOB33M | IO\_L4P\_T0\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| D9 |  | IOB33S | IO\_L6N\_T0\_VREF\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| D10 |  | IOB33S | IO\_L19N\_T3\_VREF\_16 | UNUSED |  | 16 |  |  |  |  |  |  |  |  |
| D11 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| D12 | data\_in<3> | IOB | IO\_L6P\_T0\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| D13 | data\_in<4> | IOB | IO\_L6N\_T0\_VREF\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| D14 | data\_out<1> | IOB | IO\_L1P\_T0\_AD0P\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| D15 | wr | IOB | IO\_L12P\_T1\_MRCC\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| D16 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| D17 |  | IOB33S | IO\_L16N\_T2\_A27\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| D18 |  | IOB33S | IO\_L21N\_T3\_DQS\_A18\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| E1 |  | IOB33S | IO\_L18N\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E2 |  | IOB33M | IO\_L14P\_T2\_SRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E3 |  | IOB33M | IO\_L12P\_T1\_MRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E4 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| E5 |  | IOB33S | IO\_L5N\_T0\_AD13N\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E6 |  | IOB33M | IO\_L5P\_T0\_AD13P\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E7 |  | IOB33M | IO\_L6P\_T0\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| E8 |  |  | VCCBATT\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E9 |  |  | CCLK\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E10 |  |  | TCK\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E11 |  |  | TDI\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E12 |  |  | TMS\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E13 |  |  | TDO\_0 |  |  |  |  |  |  |  |  |  |  |  |
| E14 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| E15 | fifo\_overflow | IOB | IO\_L11P\_T1\_SRCC\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| E16 | fifo\_underflow | IOB | IO\_L11N\_T1\_SRCC\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| E17 |  | IOB33M | IO\_L16P\_T2\_A28\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| E18 |  | IOB33M | IO\_L21P\_T3\_DQS\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| F1 |  | IOB33M | IO\_L18P\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| F2 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| F3 |  | IOB33S | IO\_L13N\_T2\_MRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| F4 |  | IOB33M | IO\_L13P\_T2\_MRCC\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| F5 |  | IOB33 | IO\_0\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| F6 |  | IOB33S | IO\_L19N\_T3\_VREF\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| F7 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| F8 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| F9 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| F10 |  |  | VCCBRAM |  |  |  |  |  |  |  |  |  |  |  |
| F11 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| F12 |  |  | VCCAUX |  |  |  |  |  |  |  | 1.8 |  |  |  |
| F13 | data\_in<1> | IOB | IO\_L5P\_T0\_AD9P\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| F14 | data\_in<2> | IOB | IO\_L5N\_T0\_AD9N\_15 | INPUT | LVCMOS18\* | 15 |  |  |  | NONE |  | UNLOCATED | NO | NONE |
| F15 |  | IOB33M | IO\_L14P\_T2\_SRCC\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| F16 |  | IOB33S | IO\_L14N\_T2\_SRCC\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| F17 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| F18 |  | IOB33S | IO\_L22N\_T3\_A16\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| G1 |  | IOB33S | IO\_L17N\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| G2 |  | IOB33S | IO\_L15N\_T2\_DQS\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| G3 |  | IOB33S | IO\_L20N\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| G4 |  | IOB33M | IO\_L20P\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| G5 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| G6 |  | IOB33M | IO\_L19P\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| G7 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| G8 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| G9 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| G10 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| G11 |  |  | VCCBRAM |  |  |  |  |  |  |  |  |  |  |  |
| G12 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| G13 | data\_out<0> | IOB | IO\_0\_15 | OUTPUT | LVCMOS18\* | 15 | 12 | SLOW |  |  |  | UNLOCATED | NO | NONE |
| G14 |  | IOB33S | IO\_L15N\_T2\_DQS\_ADV\_B\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| G15 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| G16 |  | IOB33S | IO\_L13N\_T2\_MRCC\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| G17 |  | IOB33S | IO\_L18N\_T2\_A23\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| G18 |  | IOB33M | IO\_L22P\_T3\_A17\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| H1 |  | IOB33M | IO\_L17P\_T2\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| H2 |  | IOB33M | IO\_L15P\_T2\_DQS\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| H3 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| H4 |  | IOB33S | IO\_L21N\_T3\_DQS\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| H5 |  | IOB33S | IO\_L24N\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| H6 |  | IOB33M | IO\_L24P\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| H7 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| H8 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| H9 |  |  | GNDADC\_0 |  |  |  |  |  |  |  |  |  |  |  |
| H10 |  |  | VCCADC\_0 |  |  |  |  |  |  |  |  |  |  |  |
| H11 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| H12 |  |  | VCCAUX |  |  |  |  |  |  |  | 1.8 |  |  |  |
| H13 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| H14 |  | IOB33M | IO\_L15P\_T2\_DQS\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| H15 |  | IOB33S | IO\_L19N\_T3\_A21\_VREF\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| H16 |  | IOB33M | IO\_L13P\_T2\_MRCC\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| H17 |  | IOB33M | IO\_L18P\_T2\_A24\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| H18 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| J1 |  |  | VCCO\_35 |  |  | 35 |  |  |  |  | 1.80 |  |  |  |
| J2 |  | IOB33S | IO\_L22N\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| J3 |  | IOB33M | IO\_L22P\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| J4 |  | IOB33M | IO\_L21P\_T3\_DQS\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| J5 |  | IOB33 | IO\_25\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| J6 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| J7 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| J8 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| J9 |  |  | VREFN\_0 |  |  |  |  |  |  |  |  |  |  |  |
| J10 |  | IPAD | VP\_0 | UNUSED |  | 0 |  |  |  |  |  |  |  |  |
| J11 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| J12 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| J13 |  | IOB33S | IO\_L17N\_T2\_A25\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| J14 |  | IOB33M | IO\_L19P\_T3\_A22\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| J15 |  | IOB33S | IO\_L24N\_T3\_RS0\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| J16 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| J17 |  | IOB33M | IO\_L23P\_T3\_FOE\_B\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| J18 |  | IOB33S | IO\_L23N\_T3\_FWE\_B\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| K1 |  | IOB33S | IO\_L23N\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| K2 |  | IOB33M | IO\_L23P\_T3\_35 | UNUSED |  | 35 |  |  |  |  |  |  |  |  |
| K3 |  | IOB33M | IO\_L2P\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| K4 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| K5 |  | IOB33M | IO\_L5P\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| K6 |  | IOB33 | IO\_0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| K7 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| K8 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| K9 |  | IPAD | VN\_0 | UNUSED |  | 0 |  |  |  |  |  |  |  |  |
| K10 |  |  | VREFP\_0 |  |  |  |  |  |  |  |  |  |  |  |
| K11 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| K12 |  |  | VCCAUX |  |  |  |  |  |  |  | 1.8 |  |  |  |
| K13 |  | IOB33M | IO\_L17P\_T2\_A26\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| K14 |  |  | VCCO\_15 |  |  | 15 |  |  |  |  | 1.80 |  |  |  |
| K15 |  | IOB33M | IO\_L24P\_T3\_RS1\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| K16 |  | IOB33 | IO\_25\_15 | UNUSED |  | 15 |  |  |  |  |  |  |  |  |
| K17 |  | IOB33M | IO\_L1P\_T0\_D00\_MOSI\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| K18 |  | IOB33S | IO\_L1N\_T0\_D01\_DIN\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| L1 |  | IOB33M | IO\_L1P\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| L2 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| L3 |  | IOB33S | IO\_L2N\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| L4 |  | IOB33S | IO\_L5N\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| L5 |  | IOB33S | IO\_L6N\_T0\_VREF\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| L6 |  | IOB33M | IO\_L6P\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| L7 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| L8 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| L9 |  |  | DXN\_0 |  |  |  |  |  |  |  |  |  |  |  |
| L10 |  |  | DXP\_0 |  |  |  |  |  |  |  |  |  |  |  |
| L11 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| L12 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| L13 |  | IOB33M | IO\_L6P\_T0\_FCS\_B\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| L14 |  | IOB33M | IO\_L2P\_T0\_D02\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| L15 |  | IOB33M | IO\_L3P\_T0\_DQS\_PUDC\_B\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| L16 |  | IOB33S | IO\_L3N\_T0\_DQS\_EMCCLK\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| L17 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| L18 |  | IOB33M | IO\_L4P\_T0\_D04\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| M1 |  | IOB33S | IO\_L1N\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| M2 |  | IOB33S | IO\_L4N\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| M3 |  | IOB33M | IO\_L4P\_T0\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| M4 |  | IOB33M | IO\_L16P\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| M5 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| M6 |  | IOB33M | IO\_L18P\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| M7 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| M8 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| M9 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| M10 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| M11 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| M12 |  |  | VCCAUX |  |  |  |  |  |  |  | 1.8 |  |  |  |
| M13 |  | IOB33S | IO\_L6N\_T0\_D08\_VREF\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| M14 |  | IOB33S | IO\_L2N\_T0\_D03\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| M15 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| M16 |  | IOB33M | IO\_L10P\_T1\_D14\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| M17 |  | IOB33S | IO\_L10N\_T1\_D15\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| M18 |  | IOB33S | IO\_L4N\_T0\_D05\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| N1 |  | IOB33S | IO\_L3N\_T0\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| N2 |  | IOB33M | IO\_L3P\_T0\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| N3 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| N4 |  | IOB33S | IO\_L16N\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| N5 |  | IOB33M | IO\_L13P\_T2\_MRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| N6 |  | IOB33S | IO\_L18N\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| N7 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| N8 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| N9 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| N10 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| N11 |  |  | VCCINT |  |  |  |  |  |  |  | 1.0 |  |  |  |
| N12 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| N13 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| N14 |  | IOB33M | IO\_L8P\_T1\_D11\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| N15 |  | IOB33M | IO\_L11P\_T1\_SRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| N16 |  | IOB33S | IO\_L11N\_T1\_SRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| N17 |  | IOB33M | IO\_L9P\_T1\_DQS\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| N18 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| P1 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| P2 |  | IOB33M | IO\_L15P\_T2\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| P3 |  | IOB33S | IO\_L14N\_T2\_SRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| P4 |  | IOB33M | IO\_L14P\_T2\_SRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| P5 |  | IOB33S | IO\_L13N\_T2\_MRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| P6 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| P7 |  |  | INIT\_B\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P8 |  |  | CFGBVS\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P9 |  |  | PROGRAM\_B\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P10 |  |  | DONE\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P11 |  |  | M2\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P12 |  |  | M0\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P13 |  |  | M1\_0 |  |  |  |  |  |  |  |  |  |  |  |
| P14 |  | IOB33S | IO\_L8N\_T1\_D12\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| P15 |  | IOB33M | IO\_L13P\_T2\_MRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| P16 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| P17 |  | IOB33M | IO\_L12P\_T1\_MRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| P18 |  | IOB33S | IO\_L9N\_T1\_DQS\_D13\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R1 |  | IOB33M | IO\_L17P\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R2 |  | IOB33S | IO\_L15N\_T2\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R3 |  | IOB33M | IO\_L11P\_T1\_SRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R4 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| R5 |  | IOB33S | IO\_L19N\_T3\_VREF\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R6 |  | IOB33M | IO\_L19P\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R7 |  | IOB33M | IO\_L23P\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R8 |  | IOB33M | IO\_L24P\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| R9 |  |  | VCCO\_0 |  |  | 0 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| R10 |  | IOB33 | IO\_25\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R11 |  | IOB33 | IO\_0\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R12 |  | IOB33M | IO\_L5P\_T0\_D06\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R13 |  | IOB33S | IO\_L5N\_T0\_D07\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R14 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| R15 |  | IOB33S | IO\_L13N\_T2\_MRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R16 |  | IOB33M | IO\_L15P\_T2\_DQS\_RDWR\_B\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R17 |  | IOB33S | IO\_L12N\_T1\_MRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| R18 |  | IOB33M | IO\_L7P\_T1\_D09\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T1 |  | IOB33S | IO\_L17N\_T2\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T2 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| T3 |  | IOB33S | IO\_L11N\_T1\_SRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T4 |  | IOB33S | IO\_L12N\_T1\_MRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T5 |  | IOB33M | IO\_L12P\_T1\_MRCC\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T6 |  | IOB33S | IO\_L23N\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T7 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| T8 |  | IOB33S | IO\_L24N\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| T9 |  | IOB33M | IO\_L24P\_T3\_A01\_D17\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T10 |  | IOB33S | IO\_L24N\_T3\_A00\_D16\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T11 |  | IOB33M | IO\_L19P\_T3\_A10\_D26\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T12 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| T13 |  | IOB33M | IO\_L23P\_T3\_A03\_D19\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T14 |  | IOB33M | IO\_L14P\_T2\_SRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T15 |  | IOB33S | IO\_L14N\_T2\_SRCC\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T16 |  | IOB33S | IO\_L15N\_T2\_DQS\_DOUT\_CSO\_B\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| T17 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| T18 |  | IOB33S | IO\_L7N\_T1\_D10\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U1 |  | IOB33M | IO\_L7P\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U2 |  | IOB33M | IO\_L9P\_T1\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U3 |  | IOB33S | IO\_L8N\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U4 |  | IOB33M | IO\_L8P\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U5 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| U6 |  | IOB33S | IO\_L22N\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U7 |  | IOB33M | IO\_L22P\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U8 |  | IOB33 | IO\_25\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U9 |  | IOB33M | IO\_L21P\_T3\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| U10 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| U11 |  | IOB33S | IO\_L19N\_T3\_A09\_D25\_VREF\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U12 |  | IOB33M | IO\_L20P\_T3\_A08\_D24\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U13 |  | IOB33S | IO\_L23N\_T3\_A02\_D18\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U14 |  | IOB33M | IO\_L22P\_T3\_A05\_D21\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U15 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| U16 |  | IOB33M | IO\_L18P\_T2\_A12\_D28\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U17 |  | IOB33M | IO\_L17P\_T2\_A14\_D30\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| U18 |  | IOB33S | IO\_L17N\_T2\_A13\_D29\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V1 |  | IOB33S | IO\_L7N\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V2 |  | IOB33S | IO\_L9N\_T1\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V3 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| V4 |  | IOB33S | IO\_L10N\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V5 |  | IOB33M | IO\_L10P\_T1\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V6 |  | IOB33S | IO\_L20N\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V7 |  | IOB33M | IO\_L20P\_T3\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V8 |  |  | VCCO\_34 |  |  | 34 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |
| V9 |  | IOB33S | IO\_L21N\_T3\_DQS\_34 | UNUSED |  | 34 |  |  |  |  |  |  |  |  |
| V10 |  | IOB33M | IO\_L21P\_T3\_DQS\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V11 |  | IOB33S | IO\_L21N\_T3\_DQS\_A06\_D22\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V12 |  | IOB33S | IO\_L20N\_T3\_A07\_D23\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V13 |  |  | GND |  |  |  |  |  |  |  |  |  |  |  |
| V14 |  | IOB33S | IO\_L22N\_T3\_A04\_D20\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V15 |  | IOB33M | IO\_L16P\_T2\_CSI\_B\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V16 |  | IOB33S | IO\_L16N\_T2\_A15\_D31\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V17 |  | IOB33S | IO\_L18N\_T2\_A11\_D27\_14 | UNUSED |  | 14 |  |  |  |  |  |  |  |  |
| V18 |  |  | VCCO\_14 |  |  | 14 |  |  |  |  | any\*\*\*\*\*\* |  |  |  |

**DETAILED REPORTS :**

**SYNTHESIS REPORT :**

Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.03 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.03 secs

--> Reading design: fifo\_mem.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Parsing

3) HDL Elaboration

4) HDL Synthesis

4.1) HDL Synthesis Report

5) Advanced HDL Synthesis

5.1) Advanced HDL Synthesis Report

6) Low Level Synthesis

7) Partition Report

8) Design Summary

8.1) Primitive and Black Box Usage

8.2) Device utilization summary

8.3) Partition Resource Summary

8.4) Timing Report

8.4.1) Clock Information

8.4.2) Asynchronous Control Signals Information

8.4.3) Timing Summary

8.4.4) Timing Details

8.4.5) Cross Clock Domains Report

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "fifo\_mem.prj"

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "fifo\_mem"

Output Format : NGC

Target Device : xc7a100t-3-csg324

---- Source Options

Top Module Name : fifo\_mem

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Shift Register Extraction : YES

ROM Style : Auto

Resource Sharing : YES

Asynchronous To Synchronous : NO

Shift Register Minimum Size : 2

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

LUT Combining : Auto

Reduce Control Sets : Auto

Add IO Buffers : YES

Global Maximum Fanout : 100000

Add Generic Clock Buffer(BUFG) : 32

Register Duplication : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Parsing \*

=========================================================================

Analyzing Verilog file "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v" into library work

Parsing module <fifo\_mem>.

Parsing module <memory\_array>.

Parsing module <read\_pointer>.

Parsing module <status\_signal>.

Parsing module <write\_pointer>.

=========================================================================

\* HDL Elaboration \*

=========================================================================

Elaborating module <fifo\_mem>.

Elaborating module <write\_pointer>.

Elaborating module <read\_pointer>.

Elaborating module <memory\_array>.

Elaborating module <status\_signal>.

WARNING:HDLCompiler:413 - "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v" Line 61: Result of 32-bit expression is truncated to fit in 1-bit target.

WARNING:HDLCompiler:413 - "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v" Line 69: Result of 32-bit expression is truncated to fit in 1-bit target.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Synthesizing Unit <fifo\_mem>.

Related source file is "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v".

Summary:

no macro.

Unit <fifo\_mem> synthesized.

Synthesizing Unit <write\_pointer>.

Related source file is "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v".

Found 5-bit register for signal <wptr>.

Found 5-bit adder for signal <wptr[4]\_GND\_2\_o\_add\_0\_OUT> created at line 105.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 5 D-type flip-flop(s).

Unit <write\_pointer> synthesized.

Synthesizing Unit <read\_pointer>.

Related source file is "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v".

Found 5-bit register for signal <rptr>.

Found 5-bit adder for signal <rptr[4]\_GND\_3\_o\_add\_0\_OUT> created at line 44.

Summary:

inferred 1 Adder/Subtractor(s).

inferred 5 D-type flip-flop(s).

Unit <read\_pointer> synthesized.

Synthesizing Unit <memory\_array>.

Related source file is "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v".

WARNING:Xst:647 - Input <wptr<4:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

WARNING:Xst:647 - Input <rptr<4:4>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Found 16x8-bit dual-port RAM <Mram\_data\_out2> for signal <data\_out2>.

Summary:

inferred 1 RAM(s).

Unit <memory\_array> synthesized.

Synthesizing Unit <status\_signal>.

Related source file is "C:\ISE Files\Major\_Project\_VLSI\fifo\_mem.v".

Found 1-bit register for signal <fifo\_underflow>.

Found 1-bit register for signal <fifo\_overflow>.

Found 4-bit subtractor for signal <wptr[3]\_rptr[3]\_sub\_1\_OUT> created at line 61.

Found 5-bit subtractor for signal <pointer\_result> created at line 62.

Summary:

inferred 2 Adder/Subtractor(s).

inferred 2 D-type flip-flop(s).

Unit <status\_signal> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# RAMs : 1

16x8-bit dual-port RAM : 1

# Adders/Subtractors : 4

4-bit subtractor : 1

5-bit adder : 2

5-bit subtractor : 1

# Registers : 4

1-bit register : 2

5-bit register : 2

# Xors : 1

1-bit xor2 : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

Synthesizing (advanced) Unit <memory\_array>.

INFO:Xst:3218 - HDL ADVISOR - The RAM <Mram\_data\_out2> will be implemented on LUTs either because you have described an asynchronous read or because of currently unsupported block RAM features. If you have described an asynchronous read, making it synchronous would allow you to take advantage of available block RAM resources, for optimized device usage and improved timings. Please refer to your documentation for coding guidelines.

-----------------------------------------------------------------------

| ram\_type | Distributed | |

-----------------------------------------------------------------------

| Port A |

| aspect ratio | 16-word x 8-bit | |

| clkA | connected to signal <clk> | rise |

| weA | connected to signal <fifo\_we> | high |

| addrA | connected to signal <wptr> | |

| diA | connected to signal <data\_in> | |

-----------------------------------------------------------------------

| Port B |

| aspect ratio | 16-word x 8-bit | |

| addrB | connected to signal <rptr> | |

| doB | connected to internal node | |

-----------------------------------------------------------------------

Unit <memory\_array> synthesized (advanced).

Synthesizing (advanced) Unit <read\_pointer>.

The following registers are absorbed into counter <rptr>: 1 register on signal <rptr>.

Unit <read\_pointer> synthesized (advanced).

Synthesizing (advanced) Unit <write\_pointer>.

The following registers are absorbed into counter <wptr>: 1 register on signal <wptr>.

Unit <write\_pointer> synthesized (advanced).

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# RAMs : 1

16x8-bit dual-port distributed RAM : 1

# Adders/Subtractors : 2

4-bit subtractor : 1

5-bit subtractor : 1

# Counters : 2

5-bit up counter : 2

# Registers : 2

Flip-Flops : 2

# Xors : 1

1-bit xor2 : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

Optimizing unit <fifo\_mem> ...

Optimizing unit <status\_signal> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block fifo\_mem, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Macro Statistics

# Registers : 12

Flip-Flops : 12

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Design Summary \*

=========================================================================

Top Level Output File Name : fifo\_mem.ngc

Primitive and Black Box Usage:

------------------------------

# BELS : 33

# GND : 1

# INV : 1

# LUT2 : 9

# LUT3 : 2

# LUT4 : 2

# LUT5 : 5

# LUT6 : 13

# FlipFlops/Latches : 12

# FDCE : 12

# RAMS : 3

# RAM32M : 1

# RAM32X1D : 2

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 24

# IBUF : 11

# OBUF : 13

Device utilization summary:

---------------------------

Selected Device : 7a100tcsg324-3

Slice Logic Utilization:

Number of Slice Registers: 12 out of 126800 0%

Number of Slice LUTs: 40 out of 63400 0%

Number used as Logic: 32 out of 63400 0%

Number used as Memory: 8 out of 19000 0%

Number used as RAM: 8

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 40

Number with an unused Flip Flop: 28 out of 40 70%

Number with an unused LUT: 0 out of 40 0%

Number of fully used LUT-FF pairs: 12 out of 40 30%

Number of unique control sets: 4

IO Utilization:

Number of IOs: 25

Number of bonded IOBs: 25 out of 210 11%

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

-----------------------------------+------------------------+-------+

Clock Signal | Clock buffer(FF name) | Load |

-----------------------------------+------------------------+-------+

clk | BUFGP | 15 |

-----------------------------------+------------------------+-------+

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -3

Minimum period: 2.375ns (Maximum Frequency: 421.070MHz)

Minimum input arrival time before clock: 1.530ns

Maximum output required time after clock: 2.071ns

Maximum combinational path delay: No path found

Timing Details:

---------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default period analysis for Clock 'clk'

Clock period: 2.375ns (frequency: 421.070MHz)

Total number of paths / destination ports: 244 / 47

-------------------------------------------------------------------------

Delay: 2.375ns (Levels of Logic = 2)

Source: top1/wptr\_3 (FF)

Destination: top3/Mram\_data\_out21 (RAM)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: top1/wptr\_3 to top3/Mram\_data\_out21

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDCE:C->Q 8 0.361 0.411 top1/wptr\_3 (top1/wptr\_3)

LUT2:I0->O 7 0.097 0.711 top4/Msub\_pointer\_result\_lut<3>1 (top4/Msub\_pointer\_result\_lut<3>)

LUT6:I1->O 3 0.097 0.289 top1/fifo\_we1 (fifo\_we)

RAM32M:WE 0.408 top3/Mram\_data\_out21

----------------------------------------

Total 2.375ns (0.963ns logic, 1.412ns route)

(40.5% logic, 59.5% route)

=========================================================================

Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 41 / 37

-------------------------------------------------------------------------

Offset: 1.530ns (Levels of Logic = 2)

Source: wr (PAD)

Destination: top3/Mram\_data\_out21 (RAM)

Destination Clock: clk rising

Data Path: wr to top3/Mram\_data\_out21

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 10 0.001 0.735 wr\_IBUF (wr\_IBUF)

LUT6:I0->O 3 0.097 0.289 top1/fifo\_we1 (fifo\_we)

RAM32M:WE 0.408 top3/Mram\_data\_out21

----------------------------------------

Total 1.530ns (0.506ns logic, 1.024ns route)

(33.1% logic, 66.9% route)

=========================================================================

Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 72 / 13

-------------------------------------------------------------------------

Offset: 2.071ns (Levels of Logic = 3)

Source: top1/wptr\_2 (FF)

Destination: fifo\_threshold (PAD)

Source Clock: clk rising

Data Path: top1/wptr\_2 to fifo\_threshold

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

FDCE:C->Q 8 0.361 0.725 top1/wptr\_2 (top1/wptr\_2)

LUT6:I0->O 1 0.097 0.511 top4/pointer\_result[4]\_pointer\_result[3]\_OR\_4\_o21 (top4/pointer\_result[4]\_pointer\_result[3]\_OR\_4\_o2)

LUT5:I2->O 1 0.097 0.279 top4/pointer\_result[4]\_pointer\_result[3]\_OR\_4\_o1 (fifo\_threshold\_OBUF)

OBUF:I->O 0.000 fifo\_threshold\_OBUF (fifo\_threshold)

----------------------------------------

Total 2.071ns (0.555ns logic, 1.516ns route)

(26.8% logic, 73.2% route)

=========================================================================

Cross Clock Domains Report:

--------------------------

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 2.375| | | |

---------------+---------+---------+---------+---------+

=========================================================================

Total REAL time to Xst completion: 4.00 secs

Total CPU time to Xst completion: 3.98 secs

-->

Total memory usage is 431144 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 4 ( 0 filtered)

Number of infos : 1 ( 0 filtered)

**TRANSLATION REPORT :**

Release 14.7 ngdbuild P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

Command Line: C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\ngdbuild.exe

-intstyle ise -dd \_ngo -nt timestamp -i -p xc7a100t-csg324-3 fifo\_mem.ngc

fifo\_mem.ngd

Reading NGO file "C:/ISE Files/Major\_Project\_VLSI/fifo\_mem.ngc" ...

Gathering constraint information from source properties...

Done.

Resolving constraint associations...

Checking Constraint Associations...

Done...

Checking expanded design ...

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

NGDBUILD Design Results Summary:

Number of errors: 0

Number of warnings: 0

Total memory usage is 213972 kilobytes

Writing NGD file "fifo\_mem.ngd" ...

Total REAL time to NGDBUILD completion: 2 sec

Total CPU time to NGDBUILD completion: 2 sec

Writing NGDBUILD log file "fifo\_mem.bld"...

**MAP REPORT :**

Release 14.7 Map P.20131013 (nt64)

Xilinx Mapping Report File for Design 'fifo\_mem'

Design Information

------------------

Command Line : map -intstyle ise -p xc7a100t-csg324-3 -w -logic\_opt off -ol

high -t 1 -xt 0 -register\_duplication off -r 4 -mt off -ir off -pr off -lc off

-power off -o fifo\_mem\_map.ncd fifo\_mem.ngd fifo\_mem.pcf

Target Device : xc7a100t

Target Package : csg324

Target Speed : -3

Mapper Version : artix7 -- $Revision: 1.55 $

Mapped Date : Fri Dec 16 18:14:14 2022

Design Summary

--------------

Number of errors: 0

Number of warnings: 28

Slice Logic Utilization:

Number of Slice Registers: 12 out of 126,800 1%

Number used as Flip Flops: 12

Number used as Latches: 0

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 35 out of 63,400 1%

Number used as logic: 27 out of 63,400 1%

Number using O6 output only: 22

Number using O5 output only: 0

Number using O5 and O6: 5

Number used as ROM: 0

Number used as Memory: 8 out of 19,000 1%

Number used as Dual Port RAM: 8

Number using O6 output only: 4

Number using O5 output only: 0

Number using O5 and O6: 4

Number used as Single Port RAM: 0

Number used as Shift Register: 0

Number used exclusively as route-thrus: 0

Slice Logic Distribution:

Number of occupied Slices: 12 out of 15,850 1%

Number of LUT Flip Flop pairs used: 35

Number with an unused Flip Flop: 27 out of 35 77%

Number with an unused LUT: 0 out of 35 0%

Number of fully used LUT-FF pairs: 8 out of 35 22%

Number of unique control sets: 5

Number of slice register sites lost

to control set restrictions: 24 out of 126,800 1%

A LUT Flip Flop pair for this architecture represents one LUT paired with

one Flip Flop within a slice. A control set is a unique combination of

clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is

over-mapped for a non-slice resource or if Placement fails.

OVERMAPPING of BRAM resources should be ignored if the design is

over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs: 25 out of 210 11%

Specific Feature Utilization:

Number of RAMB36E1/FIFO36E1s: 0 out of 135 0%

Number of RAMB18E1/FIFO18E1s: 0 out of 270 0%

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Number used as BUFGs: 1

Number used as BUFGCTRLs: 0

Number of IDELAYE2/IDELAYE2\_FINEDELAYs: 0 out of 300 0%

Number of ILOGICE2/ILOGICE3/ISERDESE2s: 0 out of 300 0%

Number of ODELAYE2/ODELAYE2\_FINEDELAYs: 0

Number of OLOGICE2/OLOGICE3/OSERDESE2s: 0 out of 300 0%

Number of PHASER\_IN/PHASER\_IN\_PHYs: 0 out of 24 0%

Number of PHASER\_OUT/PHASER\_OUT\_PHYs: 0 out of 24 0%

Number of BSCANs: 0 out of 4 0%

Number of BUFHCEs: 0 out of 96 0%

Number of BUFRs: 0 out of 24 0%

Number of CAPTUREs: 0 out of 1 0%

Number of DNA\_PORTs: 0 out of 1 0%

Number of DSP48E1s: 0 out of 240 0%

Number of EFUSE\_USRs: 0 out of 1 0%

Number of FRAME\_ECCs: 0 out of 1 0%

Number of IBUFDS\_GTE2s: 0 out of 4 0%

Number of ICAPs: 0 out of 2 0%

Number of IDELAYCTRLs: 0 out of 6 0%

Number of IN\_FIFOs: 0 out of 24 0%

Number of MMCME2\_ADVs: 0 out of 6 0%

Number of OUT\_FIFOs: 0 out of 24 0%

Number of PCIE\_2\_1s: 0 out of 1 0%

Number of PHASER\_REFs: 0 out of 6 0%

Number of PHY\_CONTROLs: 0 out of 6 0%

Number of PLLE2\_ADVs: 0 out of 6 0%

Number of STARTUPs: 0 out of 1 0%

Number of XADCs: 0 out of 1 0%

Average Fanout of Non-Clock Nets: 3.79

Peak Memory Usage: 773 MB

Total REAL time to MAP completion: 16 secs

Total CPU time to MAP completion: 12 secs

Table of Contents

-----------------

Section 1 - Errors

Section 2 - Warnings

Section 3 - Informational

Section 4 - Removed Logic Summary

Section 5 - Removed Logic

Section 6 - IOB Properties

Section 7 - RPMs

Section 8 - Guide Report

Section 9 - Area Group and Partition Summary

Section 10 - Timing Report

Section 11 - Configuration String Information

Section 12 - Control Set Information

Section 13 - Utilization by Hierarchy

Section 1 - Errors

------------------

Section 2 - Warnings

--------------------

WARNING:LIT:701 - PAD symbol "clk" has an undefined IOSTANDARD.

WARNING:LIT:702 - PAD symbol "clk" is not constrained (LOC) to a specific

location.

WARNING:PhysDesignRules:367 - The signal <top3/Mram\_data\_out21\_RAMD\_D1\_O> is

incomplete. The signal does not drive any load pins in the design.

WARNING:PhysDesignRules:2452 - The IOB clk is either not constrained (LOC) to a

specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB rd is either not constrained (LOC) to a

specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB fifo\_full is either not constrained (LOC)

to a specific location and/or has an undefined I/O Standard (IOSTANDARD).

This condition may seriously affect the device and will be an error in

bitstream creation. It should be corrected by properly specifying the pin

location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB fifo\_empty is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB wr is either not constrained (LOC) to a

specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB fifo\_overflow is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<0> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<1> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<2> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB fifo\_threshold is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<3> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<4> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<0> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<5> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<1> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<6> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB fifo\_underflow is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<2> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_out<7> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<3> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB rst\_n is either not constrained (LOC) to

a specific location and/or has an undefined I/O Standard (IOSTANDARD). This

condition may seriously affect the device and will be an error in bitstream

creation. It should be corrected by properly specifying the pin location and

I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<4> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<5> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<6> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

WARNING:PhysDesignRules:2452 - The IOB data\_in<7> is either not constrained

(LOC) to a specific location and/or has an undefined I/O Standard

(IOSTANDARD). This condition may seriously affect the device and will be an

error in bitstream creation. It should be corrected by properly specifying

the pin location and I/O Standard.

Section 3 - Informational

-------------------------

INFO:LIT:243 - Logical network top3/Mram\_data\_out222/SPO has no load.

INFO:LIT:395 - The above info message is repeated 1 more times for the following

(max. 5 shown):

top3/Mram\_data\_out221/SPO

To see the details of these info messages, please use the -detail switch.

INFO:LIT:244 - All of the single ended outputs in this design are using slew

rate limited output drivers. The delay on speed critical single ended outputs

can be dramatically reduced by designating them as fast outputs.

INFO:Pack:1716 - Initializing temperature to 85.000 Celsius. (default - Range:

0.000 to 85.000 Celsius)

INFO:Pack:1720 - Initializing voltage to 0.950 Volts. (default - Range: 0.950 to

1.050 Volts)

INFO:Map:215 - The Interim Design Summary has been generated in the MAP Report

(.mrp).

INFO:Pack:1650 - Map created a placed design.

Section 4 - Removed Logic Summary

---------------------------------

1 block(s) optimized away

Section 5 - Removed Logic

-------------------------

Optimized Block(s):

TYPE BLOCK

GND XST\_GND

Section 6 - IOB Properties

--------------------------

+---------------------------------------------------------------------------------------------------------------------------------------------------------+

| IOB Name | Type | Direction | IO Standard | Diff | Drive | Slew | Reg (s) | Resistor | IOB |

| | | | | Term | Strength | Rate | | | Delay |

+---------------------------------------------------------------------------------------------------------------------------------------------------------+

| clk | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<0> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<1> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<2> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<3> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<4> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<5> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<6> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_in<7> | IOB | INPUT | LVCMOS18 | | | | | | |

| data\_out<0> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<1> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<2> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<3> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<4> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<5> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<6> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| data\_out<7> | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| fifo\_empty | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| fifo\_full | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| fifo\_overflow | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| fifo\_threshold | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| fifo\_underflow | IOB | OUTPUT | LVCMOS18 | | 12 | SLOW | | | |

| rd | IOB | INPUT | LVCMOS18 | | | | | | |

| rst\_n | IOB | INPUT | LVCMOS18 | | | | | | |

| wr | IOB | INPUT | LVCMOS18 | | | | | | |

+---------------------------------------------------------------------------------------------------------------------------------------------------------+

Section 7 - RPMs

----------------

Section 8 - Guide Report

------------------------

Guide not run on this design.

Section 9 - Area Group and Partition Summary

--------------------------------------------

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

Area Group Information

----------------------

No area groups were found in this design.

----------------------

Section 10 - Timing Report

--------------------------

A logic-level (pre-route) timing report can be generated by using Xilinx static

timing analysis tools, Timing Analyzer (GUI) or TRCE (command line), with the

mapped NCD and PCF files. Please note that this timing report will be generated

using estimated delay information. For accurate numbers, please generate a

timing report with the post Place and Route NCD file.

For more information about the Timing Analyzer, consult the Xilinx Timing

Analyzer Reference Manual; for more information about TRCE, consult the Xilinx

Command Line Tools User Guide "TRACE" chapter.

Section 11 - Configuration String Details

-----------------------------------------

Use the "-detail" map option to print out Configuration Strings

Section 12 - Control Set Information

------------------------------------

Use the "-detail" map option to print out Control Set Information.

Section 13 - Utilization by Hierarchy

-------------------------------------

Use the "-detail" map option to print out the Utilization by Hierarchy section.

**PLACE AND ROUTE REPORT :**

Release 14.7 par P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

ADMIN-PC:: Fri Dec 16 18:14:33 2022

par -w -intstyle ise -ol high -mt off fifo\_mem\_map.ncd fifo\_mem.ncd

fifo\_mem.pcf

Constraints file: fifo\_mem.pcf.

Loading device for application Rf\_Device from file '7a100t.nph' in environment C:\Xilinx\14.7\ISE\_DS\ISE\.

"fifo\_mem" is an NCD, version 3.2, device xc7a100t, package csg324, speed -3

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)

Initializing voltage to 0.950 Volts. (default - Range: 0.950 to 1.050 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to ignore timing constraints ("par

-x"). Place and Route will run in "Performance Evaluation Mode" to automatically improve the performance of all

internal clocks in this design. Because there are not defined timing requirements, a timing score will not be

reported in the PAR report in this mode. The PAR timing summary will list the performance achieved for each clock.

Note: For the fastest runtime, set the effort level to "std". For best performance, set the effort level to "high".

Device speed data version: "PRODUCTION 1.10 2013-10-13".

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers: 12 out of 126,800 1%

Number used as Flip Flops: 12

Number used as Latches: 0

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 35 out of 63,400 1%

Number used as logic: 27 out of 63,400 1%

Number using O6 output only: 22

Number using O5 output only: 0

Number using O5 and O6: 5

Number used as ROM: 0

Number used as Memory: 8 out of 19,000 1%

Number used as Dual Port RAM: 8

Number using O6 output only: 4

Number using O5 output only: 0

Number using O5 and O6: 4

Number used as Single Port RAM: 0

Number used as Shift Register: 0

Number used exclusively as route-thrus: 0

Slice Logic Distribution:

Number of occupied Slices: 12 out of 15,850 1%

Number of LUT Flip Flop pairs used: 35

Number with an unused Flip Flop: 27 out of 35 77%

Number with an unused LUT: 0 out of 35 0%

Number of fully used LUT-FF pairs: 8 out of 35 22%

Number of slice register sites lost

to control set restrictions: 0 out of 126,800 0%

A LUT Flip Flop pair for this architecture represents one LUT paired with

one Flip Flop within a slice. A control set is a unique combination of

clock, reset, set, and enable signals for a registered element.

The Slice Logic Distribution report is not meaningful if the design is

over-mapped for a non-slice resource or if Placement fails.

OVERMAPPING of BRAM resources should be ignored if the design is

over-mapped for a non-BRAM resource or if placement fails.

IO Utilization:

Number of bonded IOBs: 25 out of 210 11%

Specific Feature Utilization:

Number of RAMB36E1/FIFO36E1s: 0 out of 135 0%

Number of RAMB18E1/FIFO18E1s: 0 out of 270 0%

Number of BUFG/BUFGCTRLs: 1 out of 32 3%

Number used as BUFGs: 1

Number used as BUFGCTRLs: 0

Number of IDELAYE2/IDELAYE2\_FINEDELAYs: 0 out of 300 0%

Number of ILOGICE2/ILOGICE3/ISERDESE2s: 0 out of 300 0%

Number of ODELAYE2/ODELAYE2\_FINEDELAYs: 0

Number of OLOGICE2/OLOGICE3/OSERDESE2s: 0 out of 300 0%

Number of PHASER\_IN/PHASER\_IN\_PHYs: 0 out of 24 0%

Number of PHASER\_OUT/PHASER\_OUT\_PHYs: 0 out of 24 0%

Number of BSCANs: 0 out of 4 0%

Number of BUFHCEs: 0 out of 96 0%

Number of BUFRs: 0 out of 24 0%

Number of CAPTUREs: 0 out of 1 0%

Number of DNA\_PORTs: 0 out of 1 0%

Number of DSP48E1s: 0 out of 240 0%

Number of EFUSE\_USRs: 0 out of 1 0%

Number of FRAME\_ECCs: 0 out of 1 0%

Number of IBUFDS\_GTE2s: 0 out of 4 0%

Number of ICAPs: 0 out of 2 0%

Number of IDELAYCTRLs: 0 out of 6 0%

Number of IN\_FIFOs: 0 out of 24 0%

Number of MMCME2\_ADVs: 0 out of 6 0%

Number of OUT\_FIFOs: 0 out of 24 0%

Number of PCIE\_2\_1s: 0 out of 1 0%

Number of PHASER\_REFs: 0 out of 6 0%

Number of PHY\_CONTROLs: 0 out of 6 0%

Number of PLLE2\_ADVs: 0 out of 6 0%

Number of STARTUPs: 0 out of 1 0%

Number of XADCs: 0 out of 1 0%

Overall effort level (-ol): High

Router effort level (-rl): High

Starting initial Timing Analysis. REAL time: 6 secs

Finished initial Timing Analysis. REAL time: 6 secs

WARNING:Par:288 - The signal top3/Mram\_data\_out21\_RAMD\_D1\_O has no load. PAR will not attempt to route this signal.

Starting Router

Phase 1 : 216 unrouted; REAL time: 7 secs

Phase 2 : 186 unrouted; REAL time: 7 secs

Phase 3 : 35 unrouted; REAL time: 7 secs

Phase 4 : 35 unrouted; (Par is working to improve performance) REAL time: 9 secs

Updating file: fifo\_mem.ncd with current fully routed design.

Phase 5 : 0 unrouted; (Par is working to improve performance) REAL time: 10 secs

Phase 6 : 0 unrouted; (Par is working to improve performance) REAL time: 10 secs

Phase 7 : 0 unrouted; (Par is working to improve performance) REAL time: 10 secs

Phase 8 : 0 unrouted; (Par is working to improve performance) REAL time: 10 secs

Phase 9 : 0 unrouted; (Par is working to improve performance) REAL time: 10 secs

Total REAL time to Router completion: 10 secs

Total CPU time to Router completion: 7 secs

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

Generating "PAR" statistics.

INFO:Par:459 - The Clock Report is not displayed in the non timing-driven mode.

Timing Score: 0 (Setup: 0, Hold: 0)

Asterisk (\*) preceding a constraint indicates it was not met.

This may be due to a setup or hold violation.

----------------------------------------------------------------------------------------------------------

Constraint | Check | Worst Case | Best Case | Timing | Timing

| | Slack | Achievable | Errors | Score

----------------------------------------------------------------------------------------------------------

Autotimespec constraint for clock net clk | SETUP | N/A| 2.446ns| N/A| 0

\_BUFGP | HOLD | 0.092ns| | 0| 0

----------------------------------------------------------------------------------------------------------

All constraints were met.

INFO:Timing:2761 - N/A entries in the Constraints List may indicate that the

constraint is not analyzed due to the following: No paths covered by this

constraint; Other constraints intersect with this constraint; or This

constraint was disabled by a Path Tracing Control. Please run the Timespec

Interaction Report (TSI) via command line (trce tsi) or Timing Analyzer GUI.

Generating Pad Report.

All signals are completely routed.

WARNING:Par:283 - There are 1 loadless signals in this design. This design will cause Bitgen to issue DRC warnings.

Total REAL time to PAR completion: 10 secs

Total CPU time to PAR completion: 7 secs

Peak Memory Usage: 666 MB

Placer: Placement generated during map.

Routing: Completed - No errors found.

Number of error messages: 0

Number of warning messages: 3

Number of info messages: 2

Writing design to file fifo\_mem.ncd

PAR done!

**POST PAR STATIC TIMING REPORT :**

--------------------------------------------------------------------------------

Release 14.7 Trace (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

C:\Xilinx\14.7\ISE\_DS\ISE\bin\nt64\unwrapped\trce.exe -intstyle ise -v 3 -s 3

-n 3 -fastpaths -xml fifo\_mem.twx fifo\_mem.ncd -o fifo\_mem.twr fifo\_mem.pcf

Design file: fifo\_mem.ncd

Physical constraint file: fifo\_mem.pcf

Device,package,speed: xc7a100t,csg324,C,-3 (PRODUCTION 1.10 2013-10-13)

Report level: verbose report

Environment Variable Effect

-------------------- ------

NONE No environment variables were set

--------------------------------------------------------------------------------

INFO:Timing:2698 - No timing constraints found, doing default enumeration.

INFO:Timing:3412 - To improve timing, see the Timing Closure User Guide (UG612).

INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths

option. All paths that are not constrained will be reported in the

unconstrained paths section(s) of the report.

INFO:Timing:3339 - The clock-to-out numbers in this timing report are based on

a 50 Ohm transmission line loading model. For the details of this model,

and for more information on accounting for different loading conditions,

please see the device datasheet.

Data Sheet report:

-----------------

All values displayed in nanoseconds (ns)

Setup/Hold to clock clk

------------+------------+------------+------------+------------+------------------+--------+

|Max Setup to| Process |Max Hold to | Process | | Clock |

Source | clk (edge) | Corner | clk (edge) | Corner |Internal Clock(s) | Phase |

------------+------------+------------+------------+------------+------------------+--------+

data\_in<0> | -0.478(R)| FAST | 2.609(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<1> | -0.496(R)| FAST | 2.617(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<2> | -0.569(R)| FAST | 2.748(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<3> | -0.524(R)| FAST | 2.634(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<4> | -0.554(R)| FAST | 2.680(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<5> | -0.497(R)| FAST | 2.619(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<6> | -0.401(R)| FAST | 2.655(R)| SLOW |clk\_BUFGP | 0.000|

data\_in<7> | -0.417(R)| FAST | 2.715(R)| SLOW |clk\_BUFGP | 0.000|

rd | -0.003(R)| FAST | 2.304(R)| SLOW |clk\_BUFGP | 0.000|

rst\_n | 0.057(R)| FAST | 1.793(R)| SLOW |clk\_BUFGP | 0.000|

wr | 0.639(R)| FAST | 2.009(R)| SLOW |clk\_BUFGP | 0.000|

------------+------------+------------+------------+------------+------------------+--------+

Clock clk to Pad

--------------+-----------------+------------+-----------------+------------+------------------+--------+

|Max (slowest) clk| Process |Min (fastest) clk| Process | | Clock |

Destination | (edge) to PAD | Corner | (edge) to PAD | Corner |Internal Clock(s) | Phase |

--------------+-----------------+------------+-----------------+------------+------------------+--------+

data\_out<0> | 8.950(R)| SLOW | 3.639(R)| FAST |clk\_BUFGP | 0.000|

data\_out<1> | 8.811(R)| SLOW | 3.554(R)| FAST |clk\_BUFGP | 0.000|

data\_out<2> | 8.966(R)| SLOW | 3.562(R)| FAST |clk\_BUFGP | 0.000|

data\_out<3> | 8.717(R)| SLOW | 3.451(R)| FAST |clk\_BUFGP | 0.000|

data\_out<4> | 8.880(R)| SLOW | 3.511(R)| FAST |clk\_BUFGP | 0.000|

data\_out<5> | 8.782(R)| SLOW | 3.466(R)| FAST |clk\_BUFGP | 0.000|

data\_out<6> | 8.629(R)| SLOW | 3.421(R)| FAST |clk\_BUFGP | 0.000|

data\_out<7> | 8.625(R)| SLOW | 3.448(R)| FAST |clk\_BUFGP | 0.000|

fifo\_empty | 8.828(R)| SLOW | 3.554(R)| FAST |clk\_BUFGP | 0.000|

fifo\_full | 9.176(R)| SLOW | 3.694(R)| FAST |clk\_BUFGP | 0.000|

fifo\_overflow | 7.654(R)| SLOW | 3.163(R)| FAST |clk\_BUFGP | 0.000|

fifo\_threshold| 8.841(R)| SLOW | 3.436(R)| FAST |clk\_BUFGP | 0.000|

fifo\_underflow| 7.807(R)| SLOW | 3.240(R)| FAST |clk\_BUFGP | 0.000|

--------------+-----------------+------------+-----------------+------------+------------------+--------+

Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 2.446| | | |

---------------+---------+---------+---------+---------+

Analysis completed Fri Dec 16 18:14:51 2022

--------------------------------------------------------------------------------

Trace Settings:

-------------------------

Trace Settings

Peak Memory Usage: 632 MB

**ISIM SIMULATOR LOG :**

ISim log file

Running: C:\ISE Files\Major\_Project\_VLSI\fifo\_tb\_isim\_beh.exe -intstyle ise -gui -tclbatch isim.cmd -wdb C:/ISE Files/Major\_Project\_VLSI/fifo\_tb\_isim\_beh.wdb

ISim P.20131013 (signature 0x7708f090)

This is a Full version of ISim.

Time resolution is 1 ps

# onerror resume

# wave add /

# run 1000 ns

Simulator is doing circuit initialization process.

Finished circuit initialization process.

**TEST BENCH REPORT :**

CODE :

`timescale 1ns / 1ps

////////////////////////////////////////////////////////////////////////////////

// Company:

// Engineer:

//

// Create Date: 16:56:39 12/16/2022

// Design Name: fifo\_mem

// Module Name: C:/ISE Files/Major\_Project\_VLSI/fifo\_tb.v

// Project Name: Major\_Project\_VLSI

// Target Device:

// Tool versions:

// Description:

//

// Verilog Test Fixture created by ISE for module: fifo\_mem

//

// Dependencies:

//

// Revision:

// Revision 0.01 - File Created

// Additional Comments:

//

////////////////////////////////////////////////////////////////////////////////

module fifo\_tb;

// Inputs

reg clk;

reg rst\_n;

reg wr;

reg rd;

reg [7:0] data\_in;

// Outputs

wire [7:0] data\_out;

wire fifo\_full;

wire fifo\_empty;

wire fifo\_threshold;

wire fifo\_overflow;

wire fifo\_underflow;

// Instantiate the Unit Under Test (UUT)

fifo\_mem uut (

.data\_out(data\_out),

.fifo\_full(fifo\_full),

.fifo\_empty(fifo\_empty),

.fifo\_threshold(fifo\_threshold),

.fifo\_overflow(fifo\_overflow),

.fifo\_underflow(fifo\_underflow),

.clk(clk),

.rst\_n(rst\_n),

.wr(wr),

.rd(rd),

.data\_in(data\_in)

);

initial begin

// Initialize Inputs

clk = 0;

rst\_n = 0;

wr = 0;

rd = 0;

data\_in = 0;

// Wait 100 ns for global reset to finish

#100 clk = 0;

rst\_n = 0;

wr = 0;

rd = 0;

data\_in = 1;

#100 clk = 0;

rst\_n = 0;

wr = 0;

rd = 1;

data\_in = 0;

#100 clk = 0;

rst\_n = 0;

wr = 0;

rd = 1;

data\_in = 1;

#100 clk = 0;

rst\_n = 0;

wr = 1;

rd = 0;

data\_in = 0;

#100 clk = 0;

rst\_n = 0;

wr = 1;

rd = 0;

data\_in = 1;

#100 clk = 0;

rst\_n = 0;

wr = 1;

rd = 1;

data\_in = 0;

#100 clk = 0;

rst\_n = 0;

wr = 1;

rd = 1;

data\_in = 1;

#100 clk = 0;

rst\_n = 1;

wr = 0;

rd = 0;

data\_in = 0;

#100 clk = 0;

rst\_n = 1;

wr = 0;

rd = 0;

data\_in = 1;

#100 clk = 0;

rst\_n = 1;

wr = 0;

rd = 1;

data\_in = 0;

#100 clk = 0;

rst\_n = 1;

wr = 0;

rd = 1;

data\_in = 1;

#100 clk = 0;

rst\_n = 1;

wr = 1;

rd = 0;

data\_in = 0;

#100 clk = 0;

rst\_n = 1;

wr = 1;

rd = 0;

data\_in = 1;

#100 clk = 0;

rst\_n = 1;

wr = 1;

rd = 1;

data\_in = 0;

#100 clk = 0;

rst\_n = 1;

wr = 1;

rd = 1;

data\_in = 1;

#100 clk = 1;

rst\_n = 0;

wr = 0;

rd = 0;

data\_in = 0;

#100 clk = 1;

rst\_n = 0;

wr = 0;

rd = 0;

data\_in = 1;

#100 clk = 1;

rst\_n = 0;

wr = 0;

rd = 1;

data\_in = 0;

#100 clk = 1;

rst\_n = 0;

wr = 0;

rd = 1;

data\_in = 1;

#100 clk = 1;

rst\_n = 0;

wr = 1;

rd = 0;

data\_in = 0;

#100 clk = 1;

rst\_n = 0;

wr = 1;

rd = 0;

data\_in = 1;

#100 clk = 1;

rst\_n = 0;

wr = 1;

rd = 1;

data\_in = 0;

#100 clk = 1;

rst\_n = 0;

wr = 1;

rd = 1;

data\_in = 1;

#100 clk = 1;

rst\_n = 1;

wr = 0;

rd = 0;

data\_in = 0;

#100 clk = 1;

rst\_n = 1;

wr = 0;

rd = 0;

data\_in = 1;

#100 clk = 1;

rst\_n = 1;

wr = 0;

rd = 1;

data\_in = 0;

#100 clk = 1;

rst\_n = 1;

wr = 0;

rd = 1;

data\_in = 1;

#100 clk = 1;

rst\_n = 1;

wr = 1;

rd = 0;

data\_in = 0;

#100 clk = 1;

rst\_n = 1;

wr = 1;

rd = 0;

data\_in = 1;

#100 clk = 1;

rst\_n = 1;

wr = 1;

rd = 1;

data\_in = 0;

#100 clk = 1;

rst\_n = 1;

wr = 1;

rd = 1;

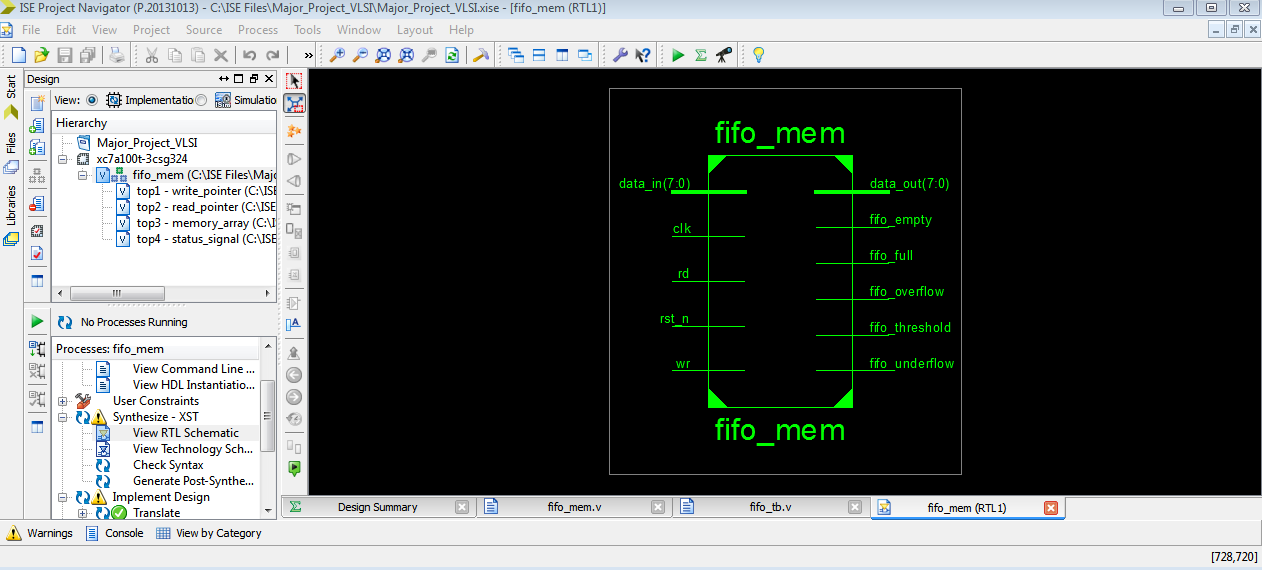
data\_in = 1;

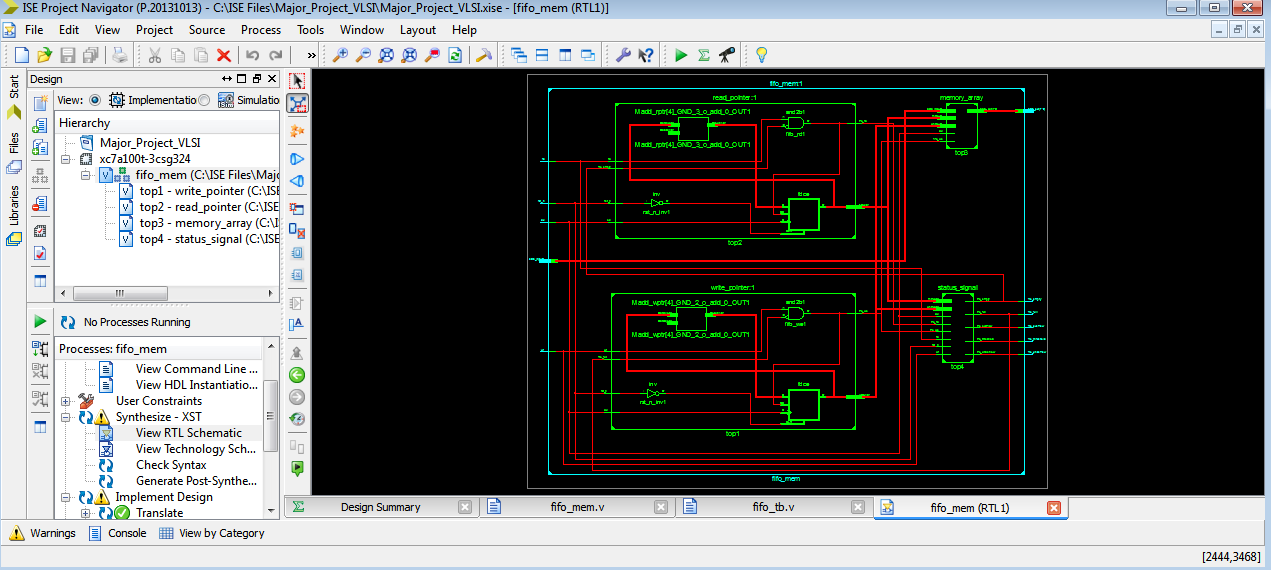
// Add stimulus here

end

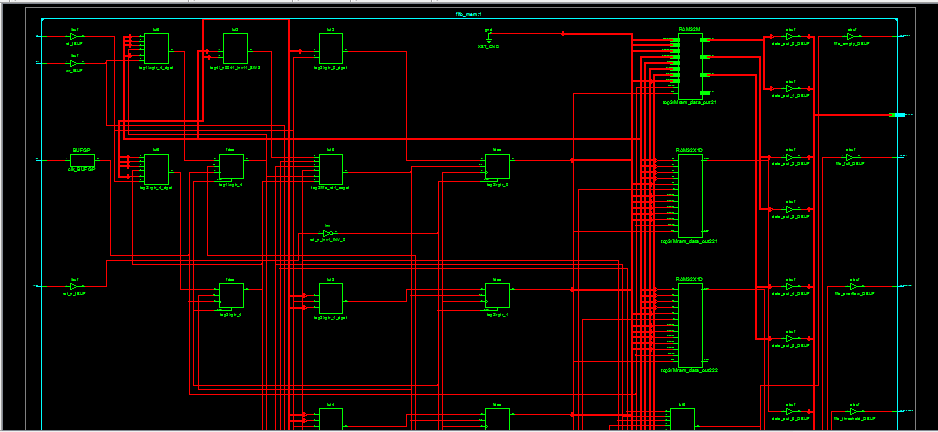
Endmodule

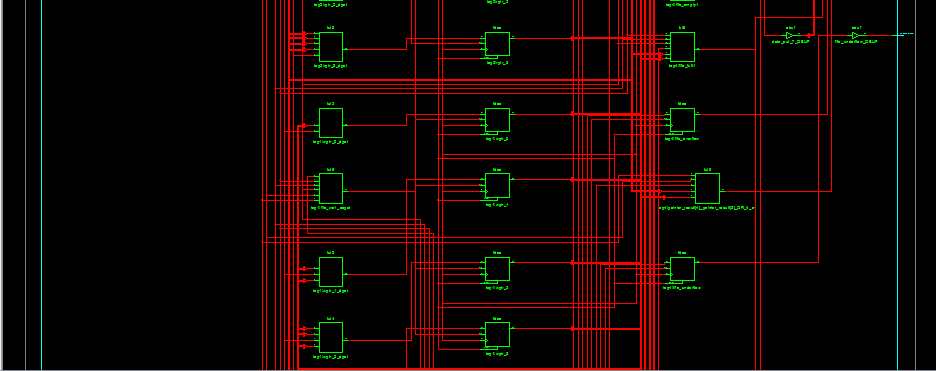
**RTL SCHEMATIC :**

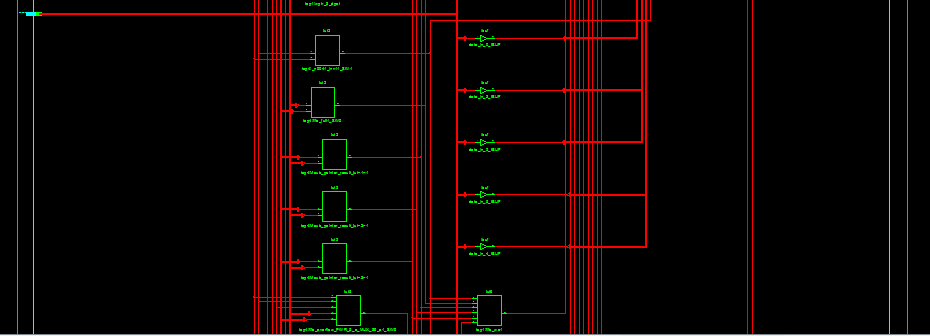


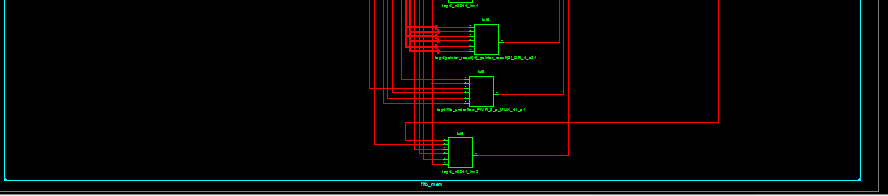


**TECHNOLOGY SCHEMATIC :**

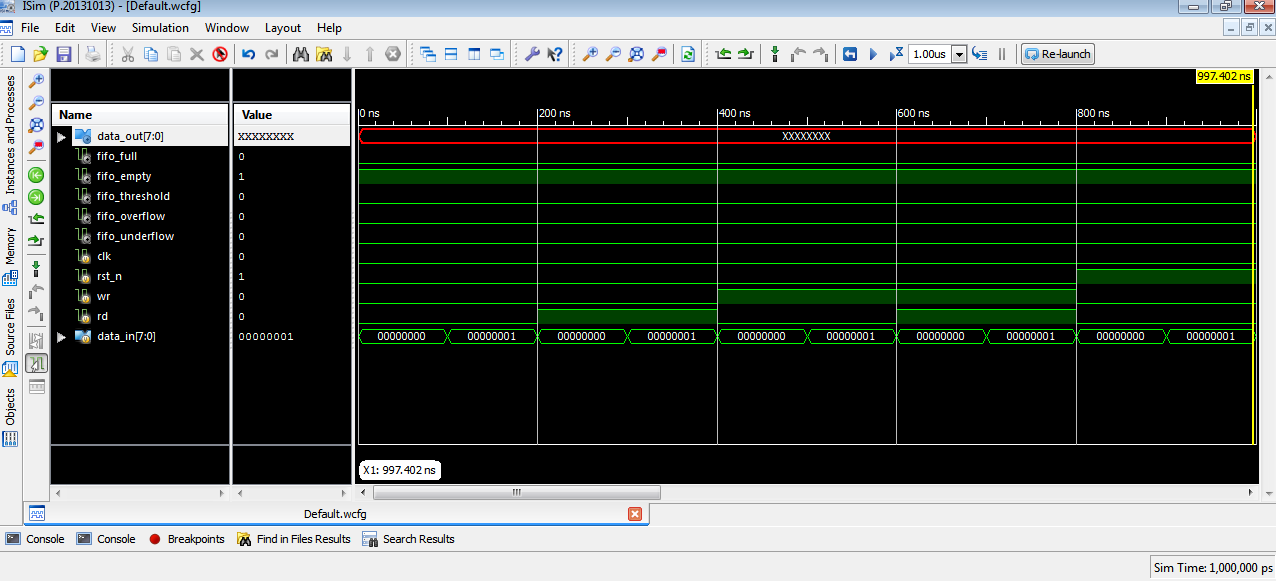








**SCHEMATIC DIAGRAM :**



**CONCLUSION :**

Thus the study and research about Synthesis and simulation of FIFO Architecture using the Verilog module in ISE project navigator software has been completed successfully by showing the schematic diagram of the FIFO along with 32 cases which was given in the Testbench. Also the RTL schematic and technology schematic of the FIFO gate has been displayed by typing the appropriate code in the Verilog module.